



## **PBA-kwaliteit en falingsrisico's: cijfers graag**

## **Apply to a production environment**

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## Overview

### **Intro tbp Electronics**

**Feed the method with effective production figures**

**Result of the analysis on production figures  
With practical examples and defined corrective actions**

**Next steps**

# Intro tbp Electronics



## Dirksland, Netherlands

- 100 Employees
- 6.000 m<sup>2</sup> production area
- 25 M€ Turn-over



## Geel, Belgium

- 330 Employees
- 30.000 m<sup>2</sup> Production area
- 75 M€ Turn-over





# Intro tbp Electronics

## tbp Dirksland (NL)

headquarters

PCBA activities

cabinet assembly

full lifecycle

low & medium volumes

high tech

## tbp Geel (BE)

PCBA activities

Cabinet assembly

full lifecycle

low up to high volumes

high tech

- Over 30 years of experience
- 100 million euros in sales
- 400 + Employees
- Operations in the Netherlands and Belgium
- Strong customer focus



# Intro tbp Electronics



Telecom



Medical



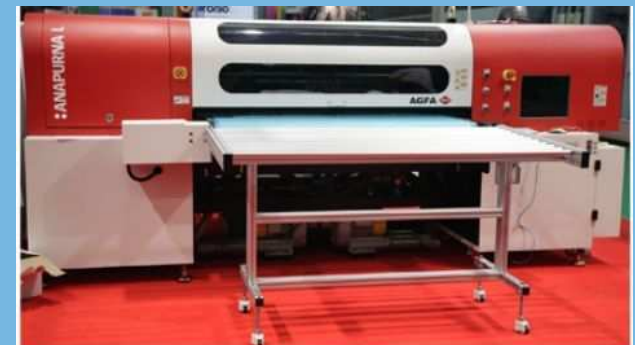
Industrial



Lighting and  
 Entertainment



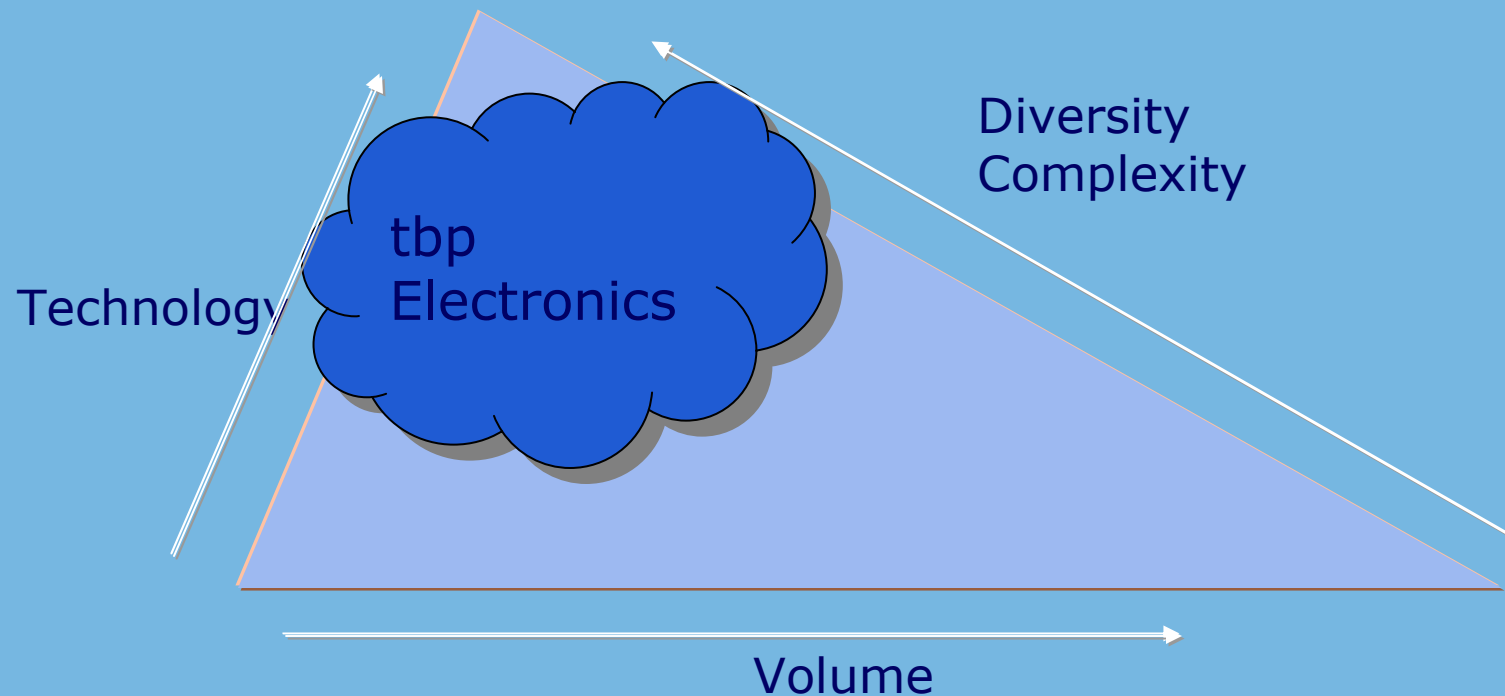
Renewable energy  
 and smart grid



Graphics

# Intro tbp Electronics

HMLV : High Mix – Low (medium) Volume





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## Measure and log

**Make track of process flow and component position over the whole process**

production  
lot



**Make a distinction between shapes and components, also in the logged results**

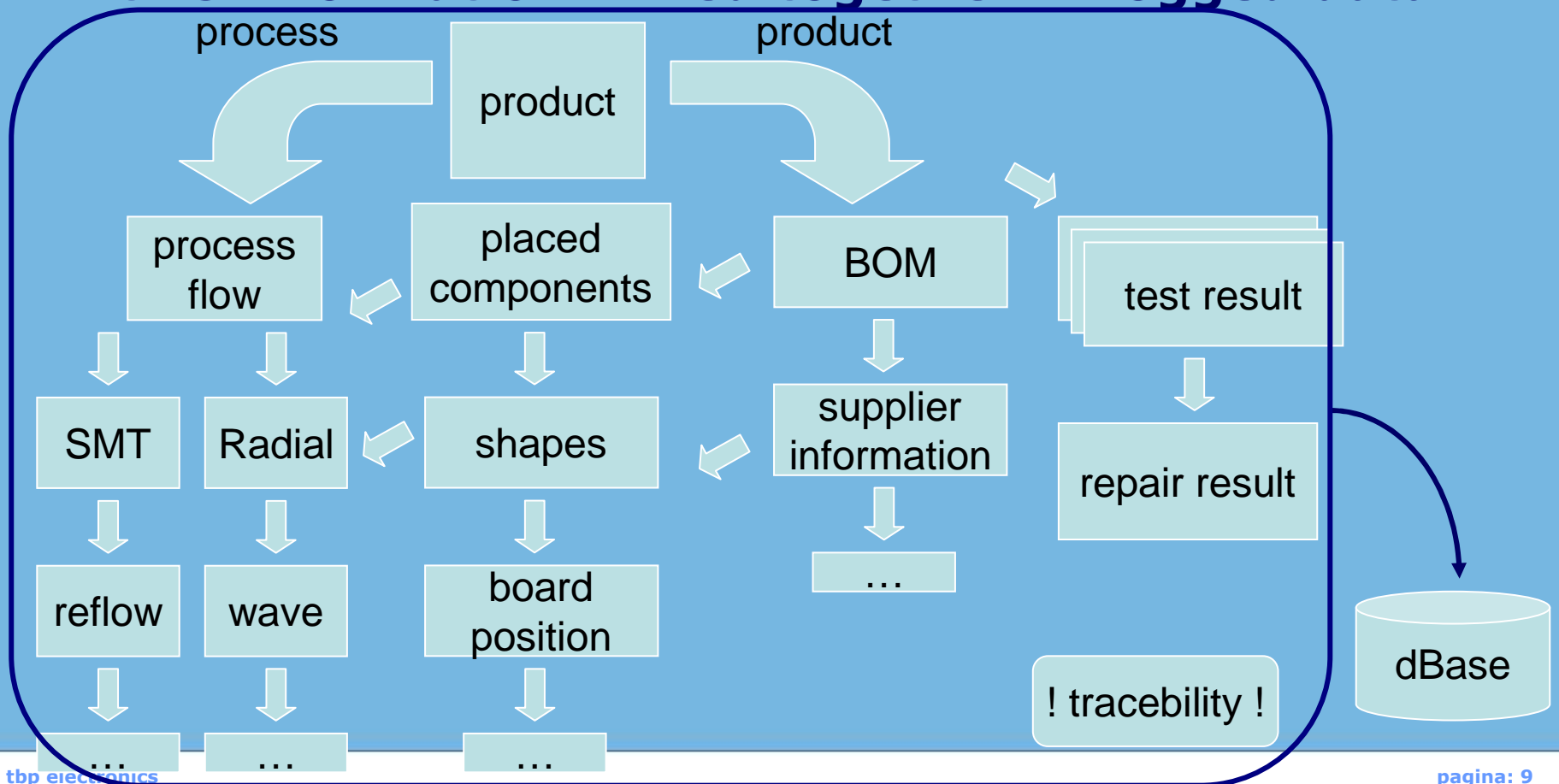
- Resistor 10k 1% -> 0603 chip
- MT47H512M4 (DDR2 SRAM) -> 63-Ball FBGA 11,5x9mm

**Declare fault types to every detected fault  
-> helps to define the root cause of the fault.**



## Measure and log

**Final result gives an overview of the product, the production process and test results. All this information linked together in logged data**





## Overview

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## Analyzed products – reflow / reflow

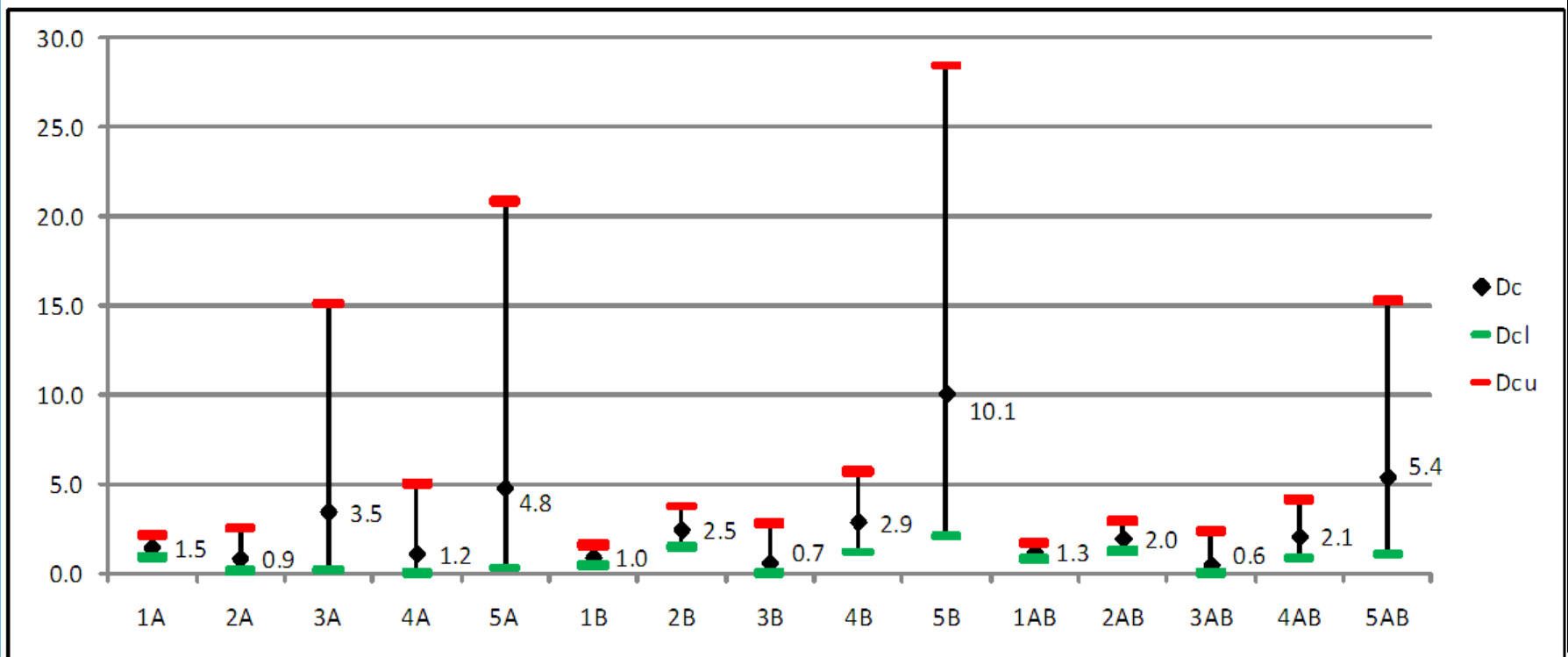
PBA info				
group name (used in DPMO graphs)		<b>A</b>	<b>B</b>	<b>AB</b>
total # components		3400	5235	-
total number of DO per PBA		20143 (≈20K)	34633 (≈35K)	-
Assembly Interconnection info				
Solder Alloy (SnPb or Pb-free)		SnPb	SnPb	SnPb
Primary Side ( <b>Top</b> )	Solder Process	Reflow	Reflow	Reflow
	Stencil Thickness	<b>150 μm</b>	<b>150 μm</b>	<b>150 μm</b>
Secondary Side ( <b>Bottom</b> )	Solder Process	Reflow	Reflow	Reflow
	Stencil Thickness	<b>150 μm</b>	<b>125 μm</b>	-
Batch info (used for DPMO analysis)				
number of batches		34	30	64
mean batch size		264	231	249
total number of PBAs		8984	6944	15928

## Example: SMT 2leaded chip - open

OPEN – Top – Reflow : A=B=AB=150µm

body size	pkg-grp	#defects	#DO	Dc	Dcl	Dcu
0402	1A	17	11,715,136	1.5	1.0	2.2
0603	2A	1	1,850,704	0.9	0.2	2.6
0805	3A	0	197,648	3.5	0.3	15.2

OPEN – Top – Reflow : A=B=AB=150µm



## Example: SMT 2leaded chip - open

SMT 2-leaded chip - OPEN - Reflow (top+bottom)  
 stencil thickness: 125/150  $\mu\text{m}$

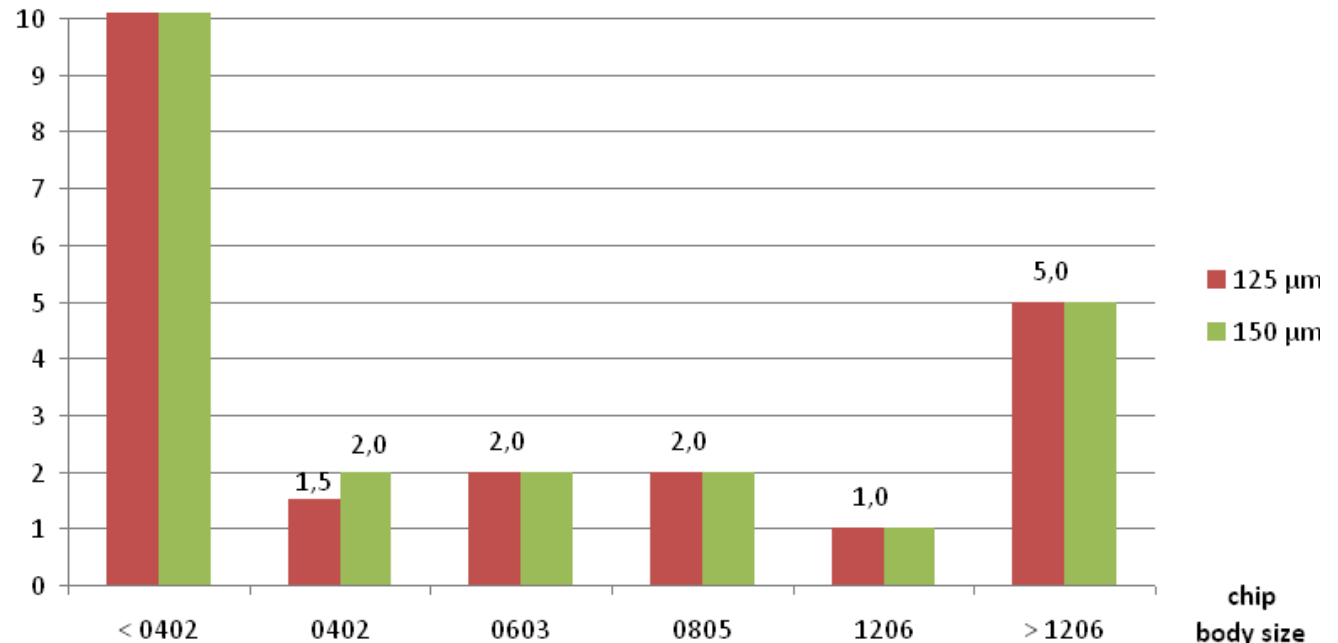
chip body size	125 $\mu\text{m}$	150 $\mu\text{m}$
< 0402	100	1000
0402	1,5	2,0
0603	2,0	2,0
0805	2,0	2,0
1206	1,0	1,0
> 1206	5,0	5,0

Color code

DPMO value = blue: based on production data PBAs

DPMO value = black: estimation

DPMO (ppm)



### •Larger components -> higher DPMO

- Pad design is typical not ideal
- Stencil should be thicker for this comp.  
 -> not allowed by other components on this board.

### •Smaller components -> same DPMO

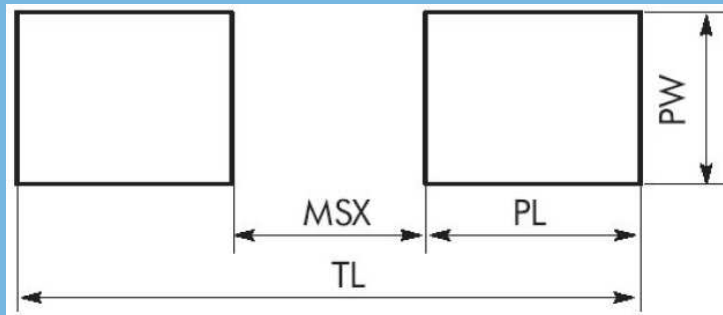
- Paste inspection
- Footprint optimization



## Example: SMT 2leaded chip - open

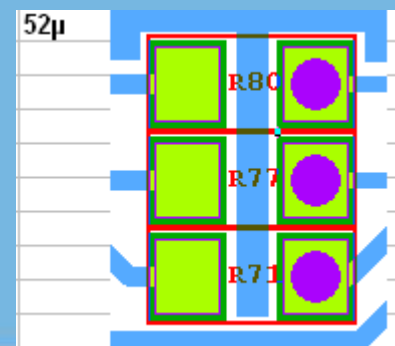
### Improvements which explains these results

- **Paste inspection + optimization of stencil**
  - 3D past inspection -> optimization of stencil process
  - Stencil adaptation
- **Footprint optimization (ex 0402)**  
 -> yield improvement of 40%



	PL	PW	MSX
<b>R0402</b>	0.47	0.558	0.51 Huidig design
	0.42	0.55	0.38 Nieuw voorstel

- **Solder mask optimization to obtain a better "dam" effect**

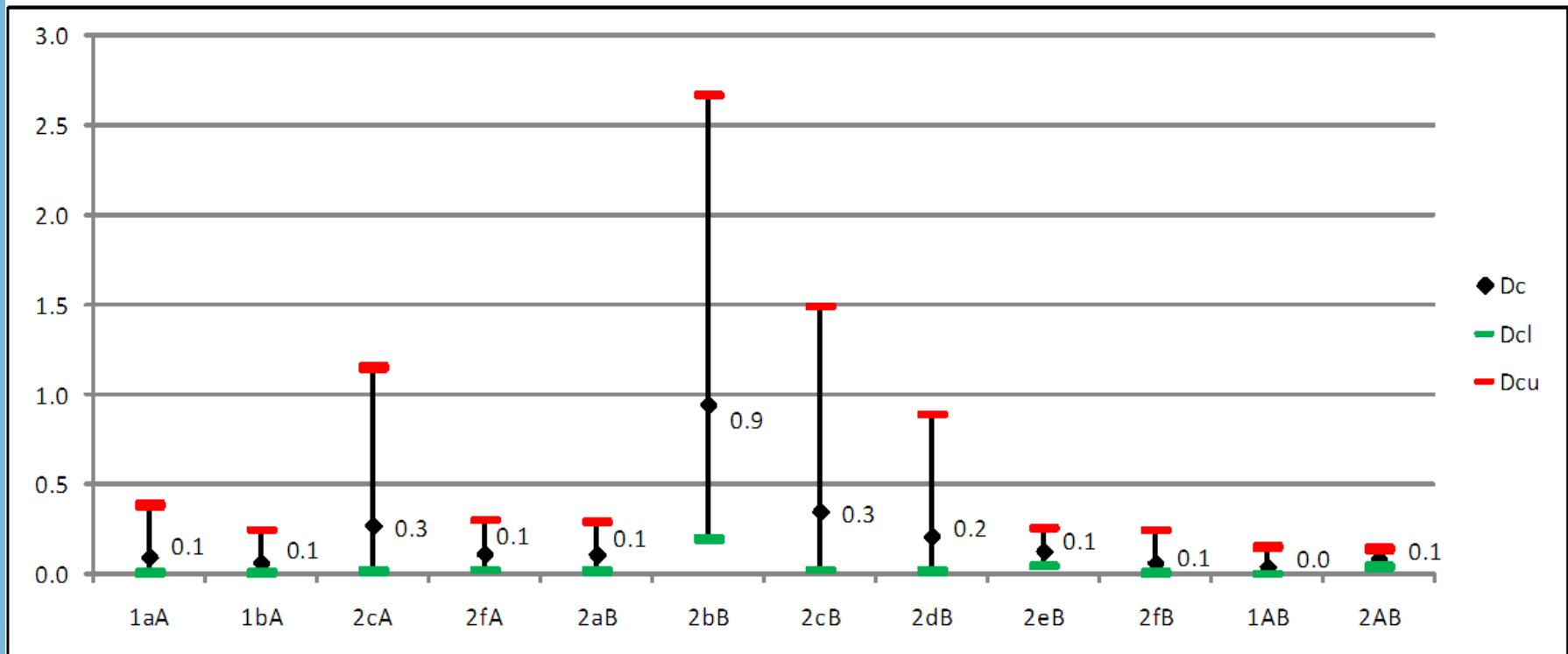


# Example: BGA - open

**OPEN – Top – Reflow : A=B=AB=150µm**

lead pitch	package type	pkg-grp	#defects	#DO	Dc	Dcl	Dcu
1.27 mm	TC = 289 / Size = 23 x 23	1aA	0	7,789,128	0.1	0.0	0.4
	TC = 676 / Size = 35 x 35	1bA	0	12,146,368	0.1	0.0	0.2
1.00 mm	TC = 289 / Size = 19 x 19	2cA	0	2,596,376	0.3	0.0	1.2
	TC = 1752 / Size = 42.5 x 42.5	2fA	1	15,739,968	0.1	0.0	0.3

**OPEN – Top – Reflow : A=B=AB=150µm**

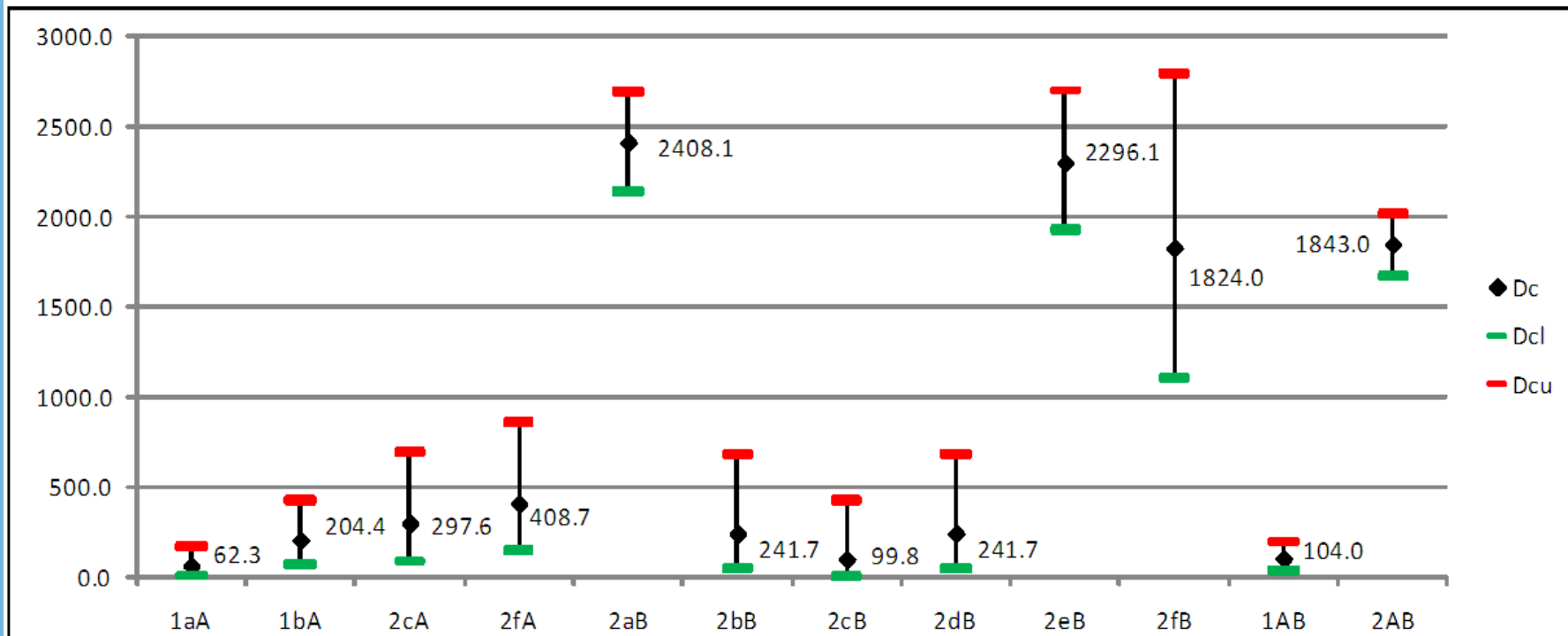


# Example: BGA – fatal defect

**FATAL DEFECT – Top – Reflow : A=B=AB=150µm**

lead pitch	package type	pkg-grp	#defects	#DO	Dc	Dcl	Dcu
1.27 mm	TC = 289 / Size = 23 x 23	1aA	1	26,952	62.3	13.2	176.0
	TC = 676 / Size = 35 x 35	1bA	3	17,968	204.4	76.0	431.4
1.00 mm	TC = 289 / Size = 19 x 19	2cA	2	8,984	297.6	91.0	700.5
	TC = 1752 / Size = 42.5 x 42.5	2fA	3	8,984	408.7	152.1	862.7
	TC = 196 / Size = 15 x 15	2aB	200	83.328	2408.1	2139.5	2698.2

**FATAL DEFECT – Top – Reflow : A=B=AB=150µm**



## Example: BGA – fatal defect

### **15x15mm 196p 1.00mm pitch**

- **Analog device which is functional critical in the product**

- improvement of test at manufacturer

- **Higher DPMO not because of production faults**

### **31x31mm 721p 1.00mm pitch**

- **Analog device with very bad structural test access (ICT, JTAG, ...)**

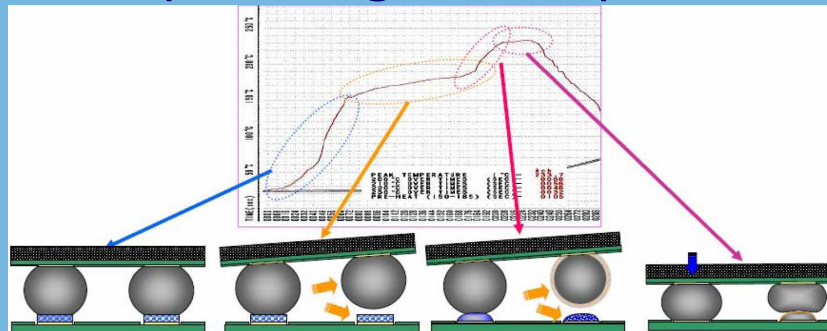
- DPMO at open/short is very low
- -> slip through to functional test
- -> bad diagnosis (open/shorts reported as fatal defects)  
-> count back to open/short gives +1 DPMO

## Example: BGA – Fatal defect

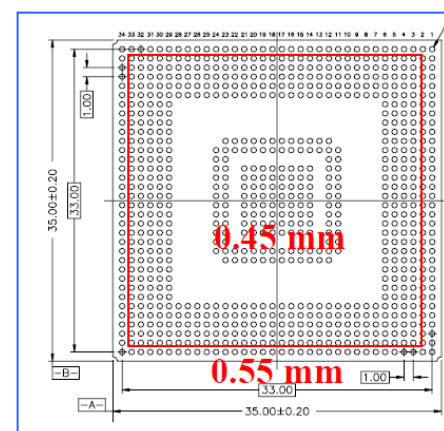
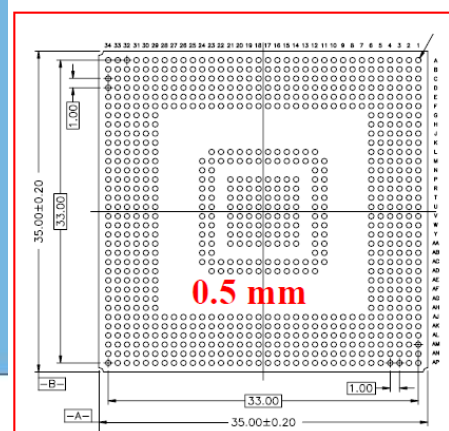


**42,5x42,5mm 1752p 1.00mm pitch**

- Defects mainly at corner of BGA (visual check)
- > Warpage / Pillowing -> BGA package structure
  - Use of anti-pillowing solder paste



- More paste on corners of BGA





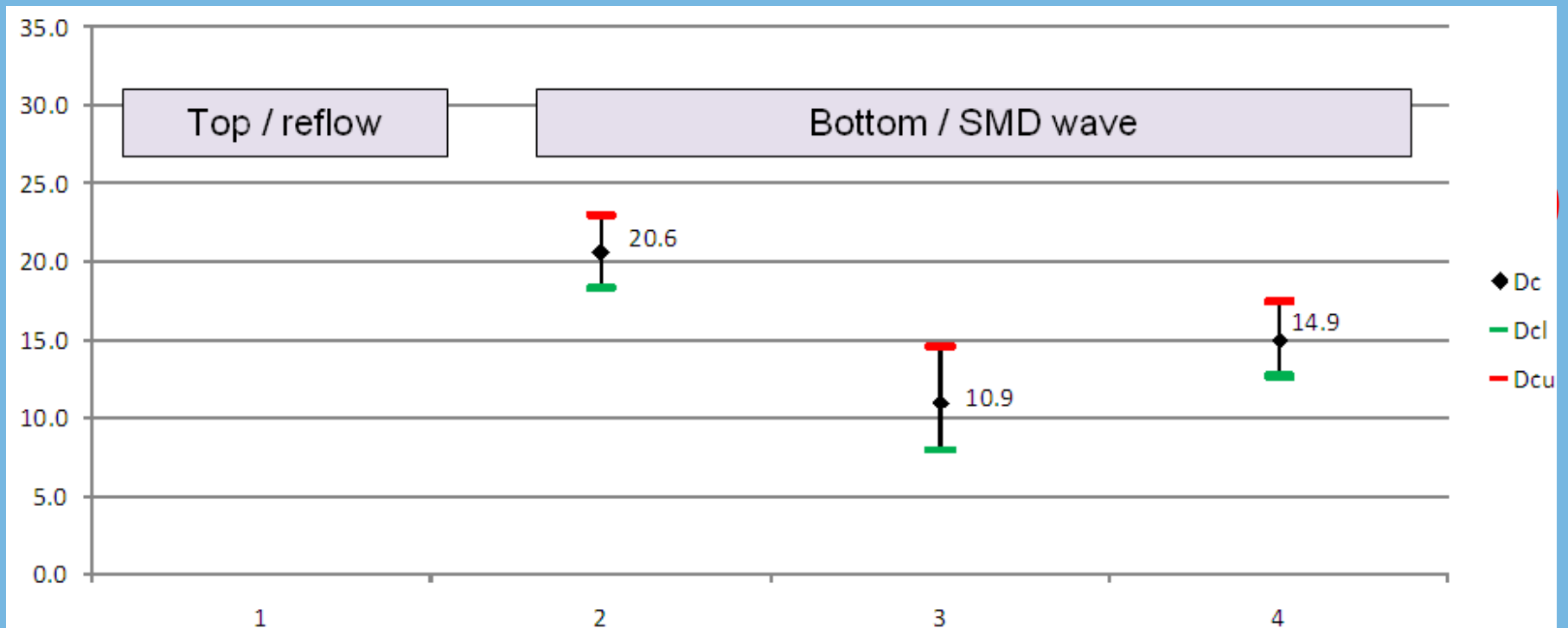
## Analyzed product – reflow / wave

PBA info		
group name (used in DPMO graphs)		C
total # components		1061
total number of DO per PBA		5202 (≈5K)
Assembly Interconnection info		
Solder Alloy (SnPb or Pb-free)		SnPb
Primary Side (Top)	Solder Process	Reflow
	Stencil Thickness	150 μm
Secondary Side (Bottom)	Solder Process	Wave
	Stencil Thickness	n.a.
Batch info (used for DPMO analysis)		
number of batches		54
mean batch size		262
total number of PBAs		14158

## Example: SMT 2-leaded chip: open

### OPEN – Top/Bottom : C=150µm (top)

body size	pkg-grp	top/bottom	#defects	#DO	Dc	Dcl	Dcu
0402	1	top / reflow	8	28,316	306.1	165.8	509.7
0603	2	bottom / SMD wave	209	10,193,760	20.6	18.3	23.0
0805	3	bottom / SMD wave	29	2,718,336	10.9	7.9	14.5
1206	4	bottom / SMD wave	104	7,022,368	14.9	12.6	17.4

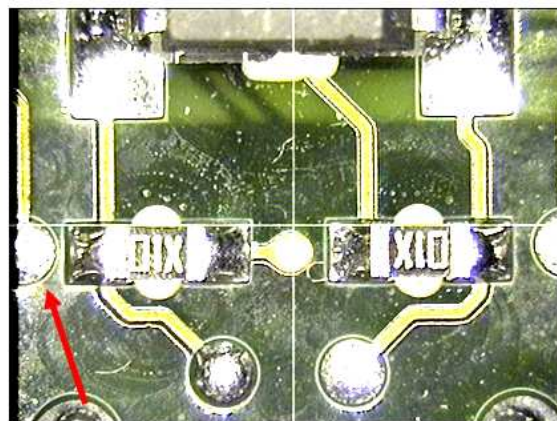
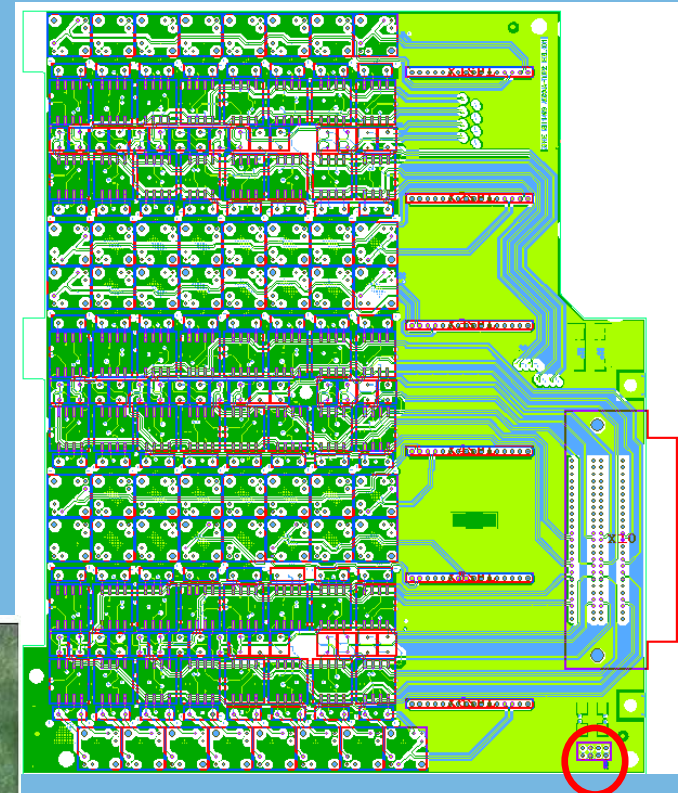


## Example: SMT 2-leaded chip: open

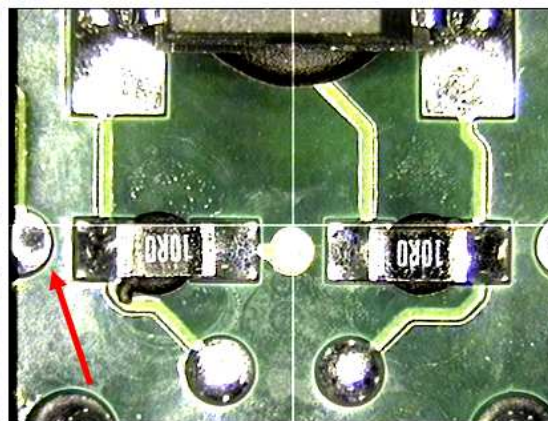
Only 1x 0402 comp at top with unlucky board position

### Wave DPMO 10x > reflow

- Small comp > risk for glue at pads
- No in process correction due to glue
- Bigger components > bad wave contact
- Pad – pad / pad – test point clearance



oud design: 200µm



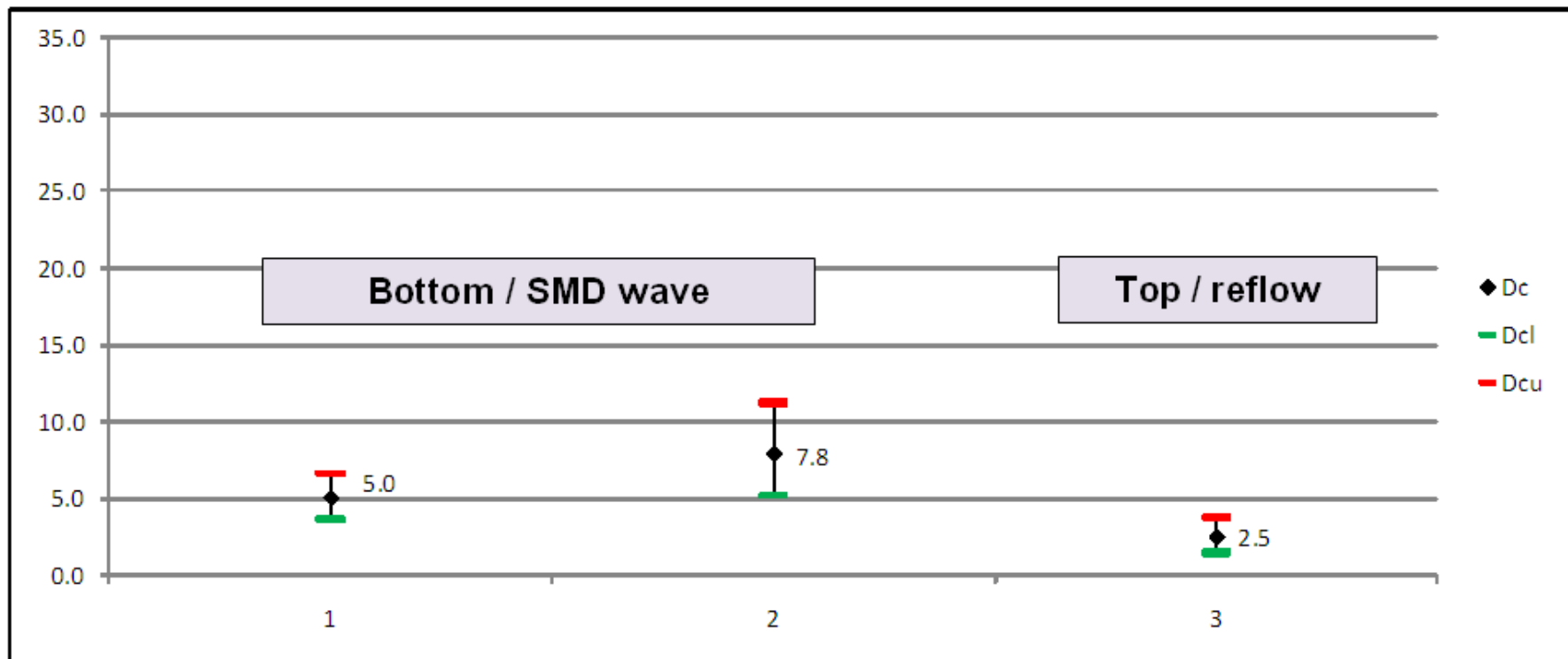
new design: 400µm

# Example: Gull-wing & flat-lead: open

OPEN – Top/Bottom : C=150µm (top)

#leads	package style	pkg-grp	top/bottom	#defects	#DO	Dc	Dcl	Dcu
<=7	DSO-G	1	bottom / SMD wave	30	6,116,256	5.0	3.7	6.7
>7	DSO-G	2	bottom / SMD wave	18	2,378,544	7.8	5.2	11.2
	DIP-F	3	top / reflow	13	5,436,672	2.5	1.6	3.8

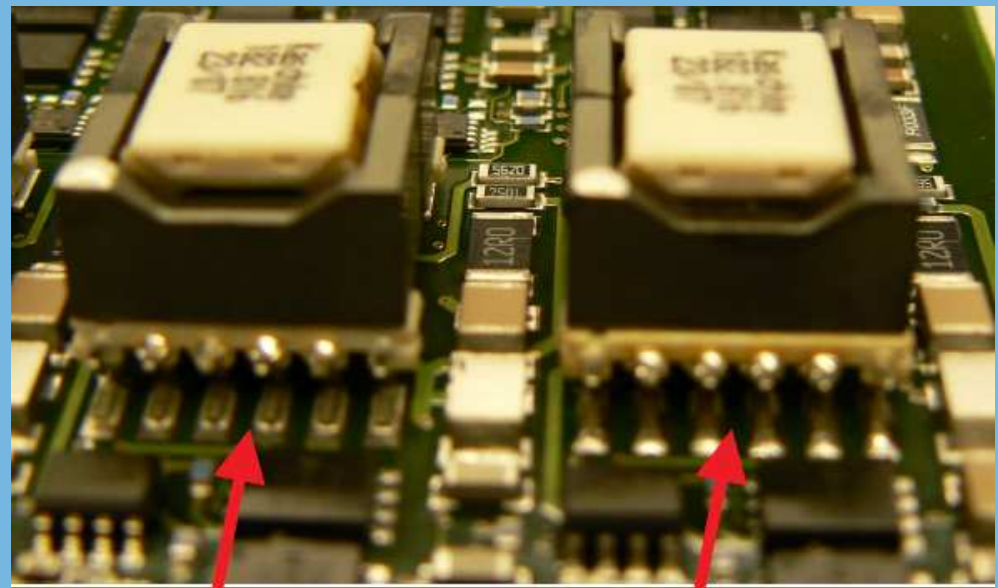
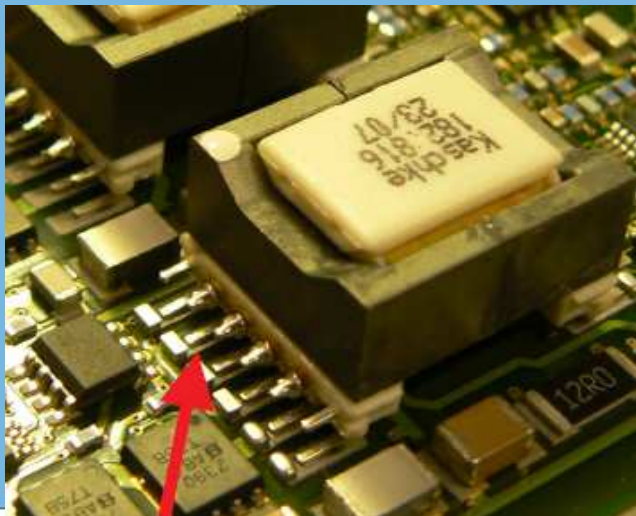
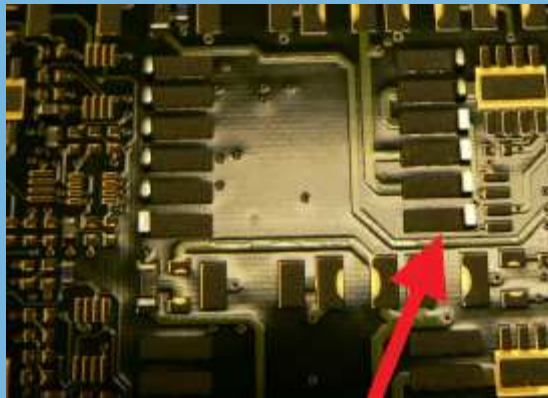
OPEN – Top/Bottom : C=150µm (top)





## Example: Gull-wing & flat-lead: open

**Good SMD result on transo's with bad copla leads  
- By use of solder preforms**



zonder preforms

Met preforms





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## Next steps

### **Know the effective quality of these topics at product AND process**

- Standardized method

### **Predict yield of products is very complex because of impact of**

- Product design
- Component selection
- Process capability

### **Actual method requires**

- A lot of data > high volume products
- Consumes time and effort

### **Move to a continuous improvement system**



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