IPC Reliability Forum: Emerging Technologies | 27–28 June, 2017 | Dusseldorf, Germany

# PHYSICS OF FAILURE BASED QUANTIFICATION OF LIFE TIME FOR ELECTRONICS BOARD ASSEMBLIES

BART VANDEVELDE, RIET LABIE, FRANCO ZANON, GEERT WILLEMS

# OUTLINE

1. The PoF vs. the statistical approach for reliability prediction

2. Practical Models based on analytical equations:
    - Via fatigue model: an alternative for IPC Engelmaier model
    - Solder fatigue of components on PCB's
    - Al Capacitor failures

3. Alternative PoF based testing approaches
    - Shock resistance of solder interconnects
    - 4pt bending instead of thermal cycling

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# STATISTICAL VS. POF APPROACH FOR LIFE TIME PREDICTION

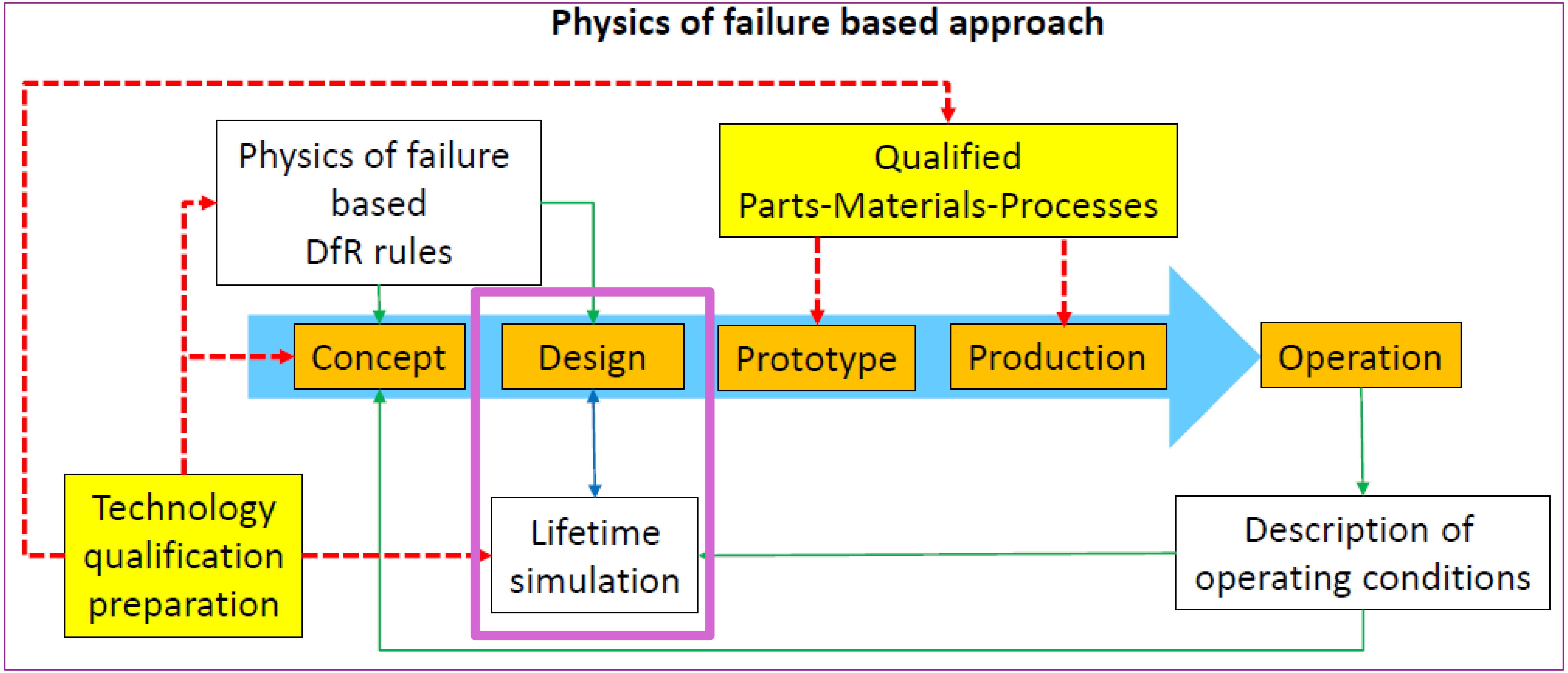
**(Pure) Statistical approach**

- Based on historical (even >15 years old) failure rate data
- Assumes constant failure rate (MTBF): models only random failure types
- Tools:
  - MIL-HDBK-217
  - Fides
  - IEC TR 62380 (Reliability data handbook)

**Physics of Failure approach**

- Predicts wear-out failures (third part of bath tub curve)
- Analysis of loads and stresses in an application and evaluating the ability of materials to endure them from a strength and mechanics material point of view
- Tools:
  - Analytical models (e.g. cEDM Via Failure and Delamination)
  - Virtual prototyping (e.g. FEM simulation, CFD, spice, etc.)
  - Engineering tool such as Sherlock

# WHERE DOES POF BASED DESIGN FOR RELIABILITY FITS INTO THE NPI (NEW PRODUCT INTEGRATION) PROCESS?



We promote to the industry this PoF based approach for designing new products.

# DIFFERENT APPROACHES OF POF BASED RELIABILITY STUDIES

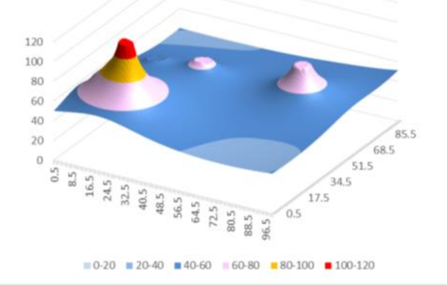
Analytical equations of simplified structures

$$T(r) = T_{amb} + C_1 I_0\left(\sqrt{\frac{2h}{kt}}\cdot r\right) + C_2 K_0\left(\sqrt{\frac{2h}{kt}}\cdot r\right)$$

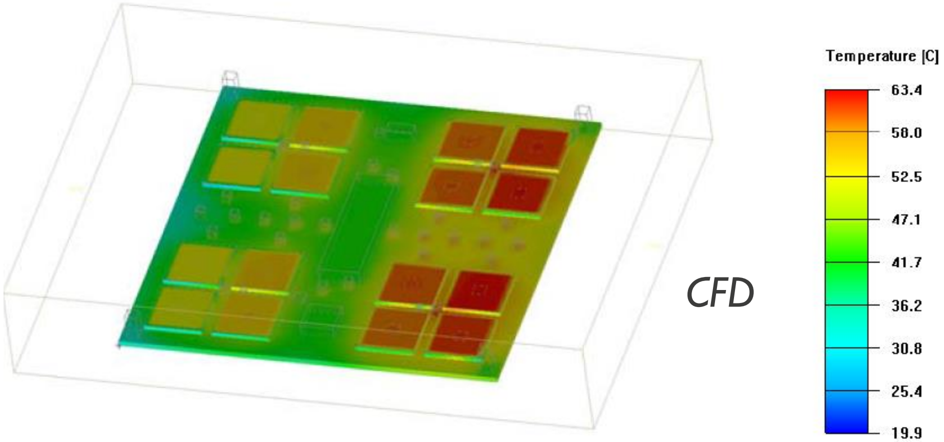
$$C_1 = \frac{-q_{in}}{k\sqrt{A}}\left[\frac{K_1\left(\sqrt{A}\cdot R_2\right)}{I_1\left(\sqrt{A}\cdot R_1\right)\cdot K_1\left(\sqrt{A}\cdot R_2\right) - K_1\left(\sqrt{A}\cdot R_1\right)\cdot I_1\left(\sqrt{A}\cdot R_2\right)}\right]$$

$$C_2 = \frac{-q_{in}}{k\sqrt{A}}\left[\frac{I_1\left(\sqrt{A}\cdot R_2\right)}{I_1\left(\sqrt{A}\cdot R_1\right)\cdot K_1\left(\sqrt{A}\cdot R_2\right) - K_1\left(\sqrt{A}\cdot R_1\right)\cdot I_1\left(\sqrt{A}\cdot R_2\right)}\right]$$

spreadsheets

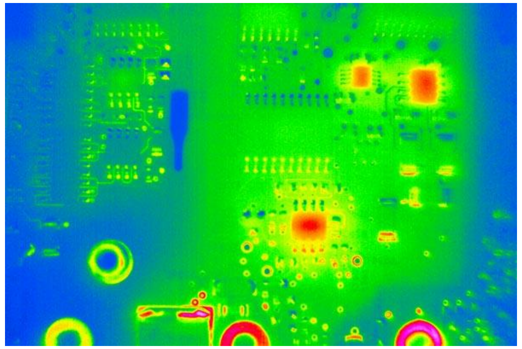


Simulations with advanced tools (CFD, FEM)



*CFD*

Experiments on test structures



*IR measurement*

# DIFFERENT APPROACHES OF POF BASED RELIABILITY STUDIES (2)

| | Level of acceptance | Time to result |
|---|---|---|
| Analytical equations of simplified structures | Low | <1 min |
| Simulations with advanced tools (CFD, FEM) | Middle | 1 week |
| Experiments on test structures | High | >1 month |

# DIFFERENT APPROACHES OF POF BASED RELIABILITY STUDIES (3)

Analytical equations of simplified structures

The corner joint gets the highest vertical tensile force, due to the upward warpage of the component

Simulations with advanced tools (CFD, FEM)

Stress distribution shows highest stresses in the corner joints

Experiments on test structures

It fails after 1219 temperature cycles

Output

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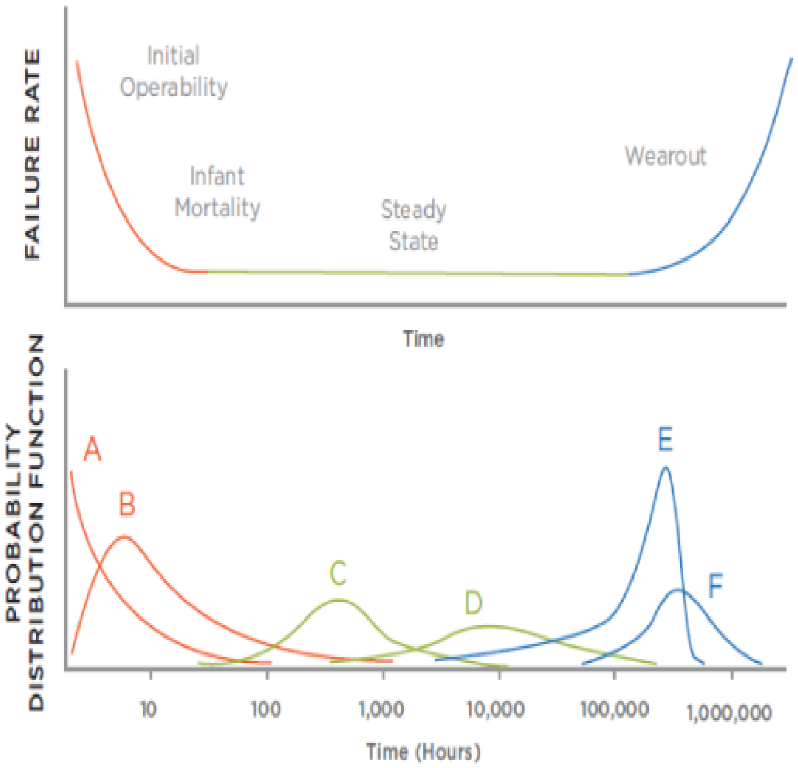
# MAJOR FAILURE MODES

## LITERATURE AND OWN STATISTICS

**Failure modes of a micro-inverter for solar applications**

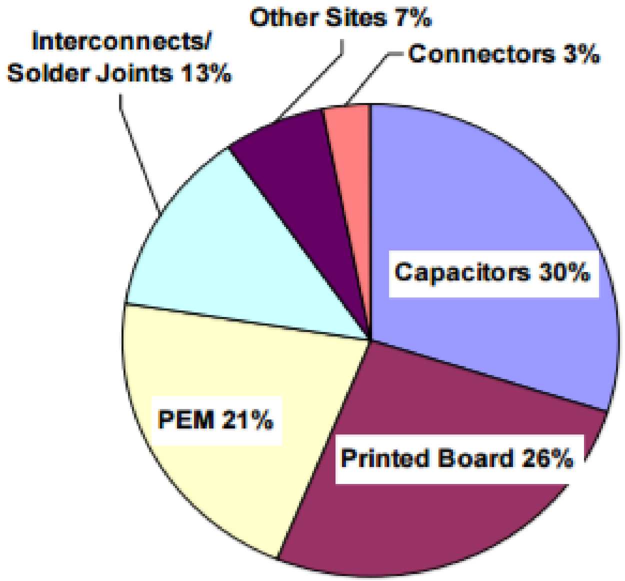


Infant Mortality:
A. Weak Solder Joints
B. Cracked Ceramic Capacitor

Steady State:
C. FET Single Event Burnout
D. Corrosion

Wearout:
E. Electrolytic Capacitor Degradation
F. Non Compliant Solder Joints (BGA,etc.)

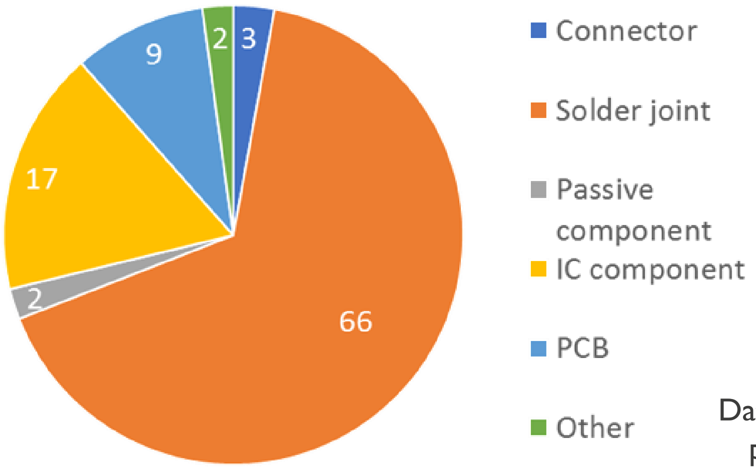
*Sinapis, K. and Folkerts,W., MLPM Benchmark Report 2013*



**CALCE** Laboratory Services reviewed 150 root-cause analyses of failures during qualification or at a customer site – Representative of over 80 different companies

*Sood, B., Root-Cause Failure Analysis of Electronics, SMTA 2013*

*% distribution of Failure studies by cEDM (imec)*

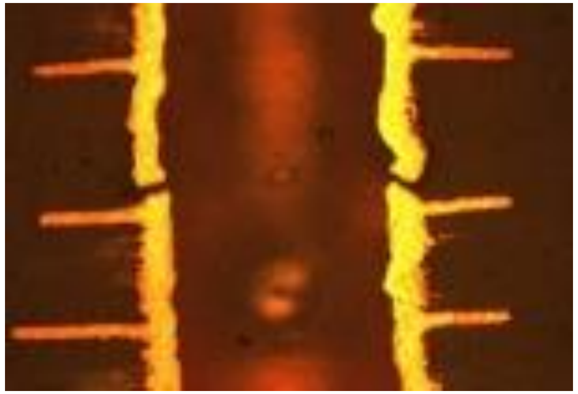


Data extracted for the period 2014-2016

# VIA FATIGUE MODEL

# VIA FATIGUE FOR PRINTED CIRCUIT BOARDS

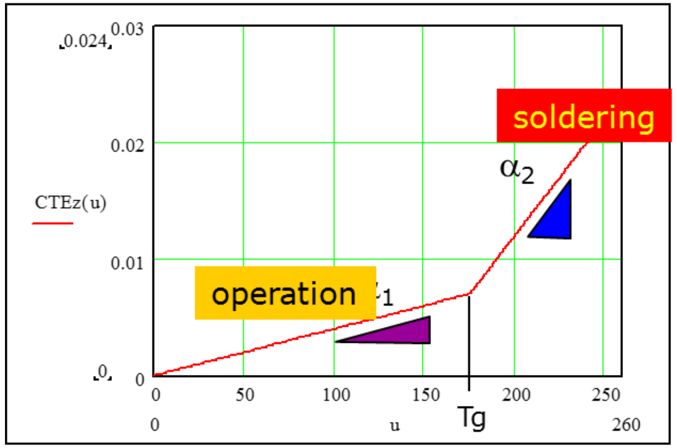
- Fracture of Cu via after temperature cycling



- Driving force: Difference in CTE between laminate and Cu-plating of via

Physical parameters driving the damage of the via

- $CTE_{FR4} – CTE_{CU}$
- $\Delta T$



Design parameters:

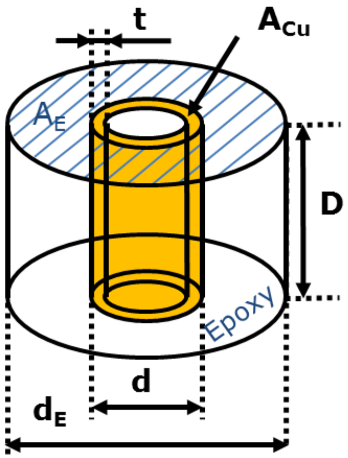
- Via diameter
- PCB thickness
- Metallisation thickness
- Inner layers

# VIA FATIGUE MODEL

## AN ALTERNATIVE FOR IPC ENGELMAIER MODEL

- Engelmaier's 2-beam model (*IPC-D-279*)

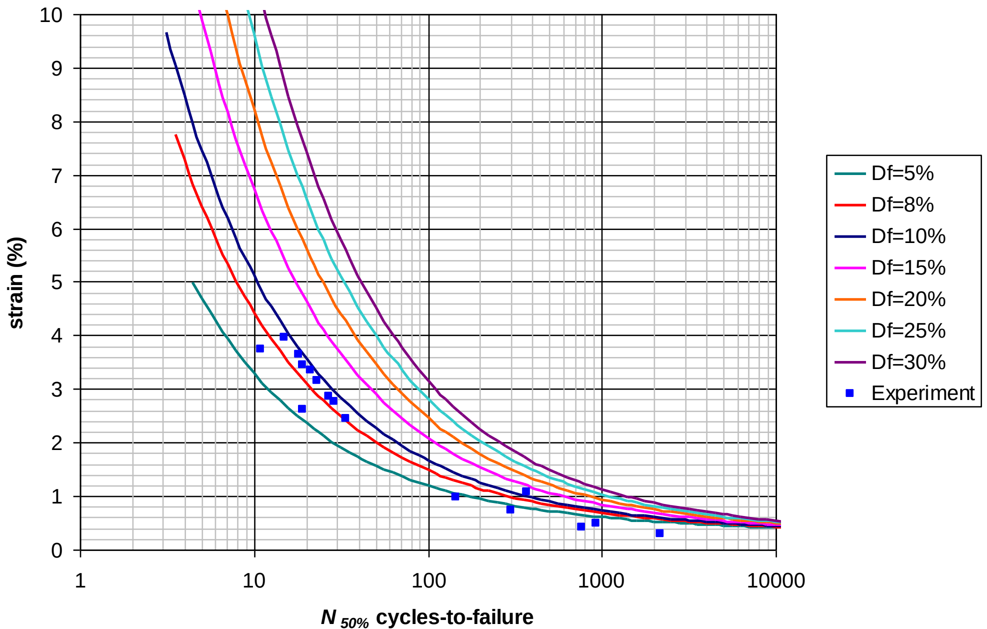
$$\Delta\varepsilon_{Cu,z} = \frac{FE_E(\Delta T) - FE_{Cu}(\Delta T)}{1 + \frac{A_{Cu}}{A_E}\frac{E_{Cu}}{E_E}}$$



$$N_f^{-0.6}D_f^{0.75} + 0.9\frac{S_u}{E}\left[\frac{\exp(D_f)}{0.36}\right]^{0.1785\log\frac{10^5}{N_f}} - \Delta\varepsilon = 0$$

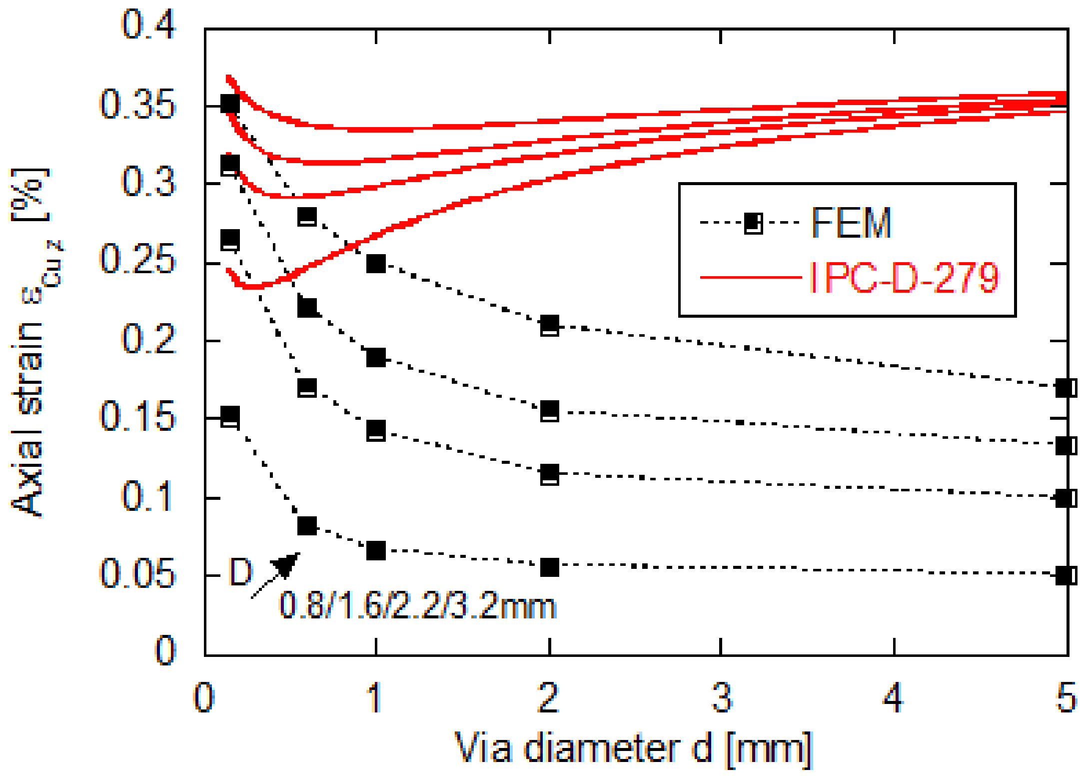
- Imec's model

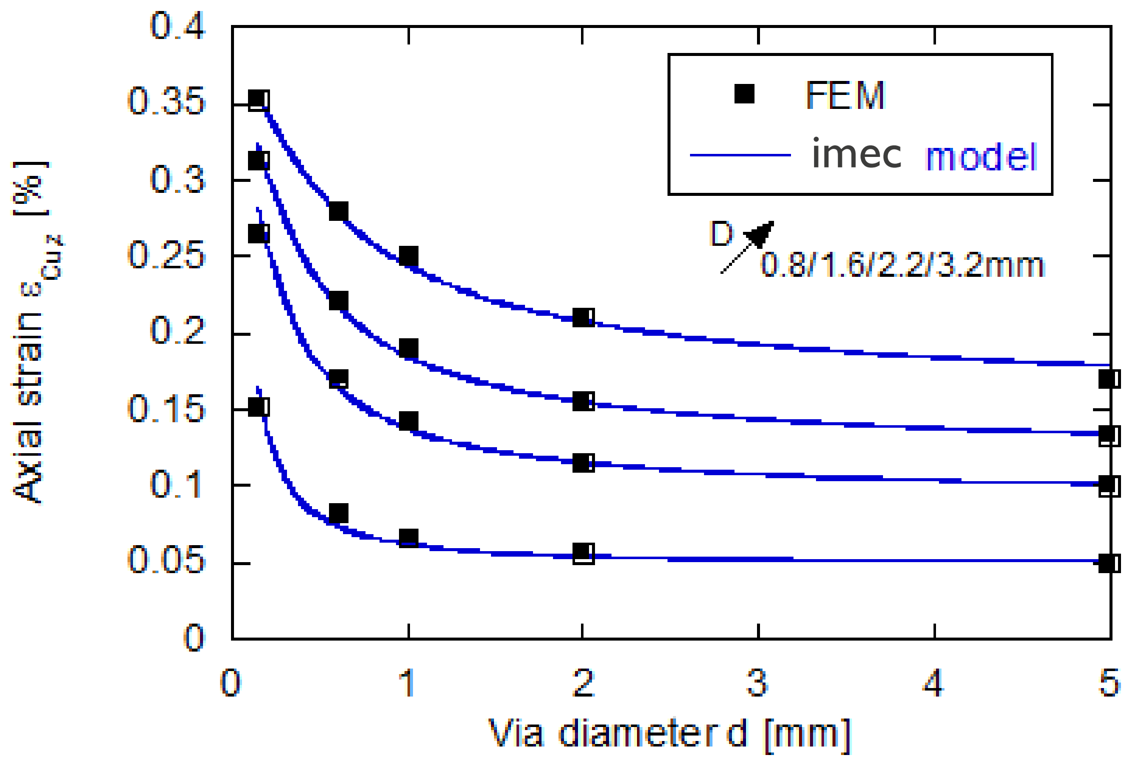
$$\Delta\varepsilon_{Cu,z} = \frac{FE_{E,z}(\Delta T) - FE_{Cu,z}(\Delta T)}{1 + \frac{A_{Cu,z}}{\boxed{A_{E,z}}}\frac{E_{Cu}}{E_z}\boxed{\frac{E_{Cu} + (1-\nu_{Cu}^2)E_{xy}}{(1-\nu_{Cu}^2)E_{Cu} + (1+\nu_{Cu})^2(1+2\nu_{Cu})E_{xy}}}}$$



# EXAMPLE CASE

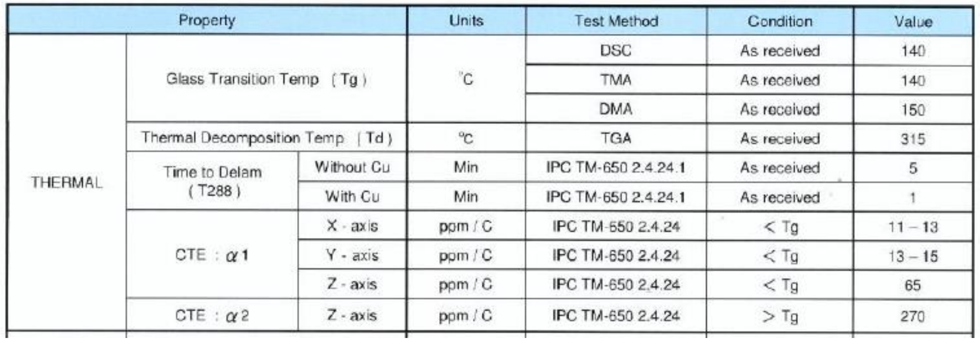
## FR4 SUBSTRATE WITH EPOXY PARAMETERS $E_{E,R}$=17GPA, $E_{E,Z}$=3GPA, $A_{E,R}$=18PPM/°C AND $FE_{E,Z}$=50PPM/°C, PLATING THICKNESS $T$ IS 20UM, ΔT=120°C





# TESTIMONY ON THE USE OF THE POF BASED **VIA FATIGUE** CALCULATOR

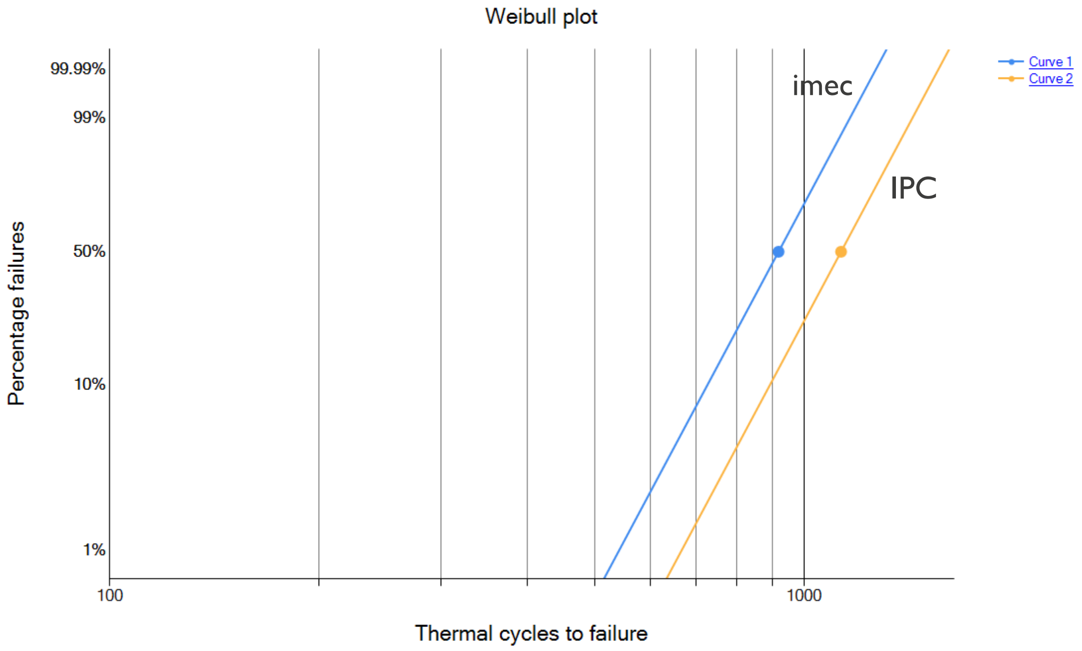
- Issues with PTH via cracking on a low cost test board meant for testing solder joint reliability of QFN's (failures at 900 cycles)



| Property | | | Units | Test Method | Condition | Value |
|---|---|---|---|---|---|---|
| THERMAL | Glass Transition Temp ( Tg ) | | °C | DSC | As received | 140 |
| | | | | TMA | As received | 140 |
| | | | | DMA | As received | 150 |
| | Thermal Decomposition Temp ( Td ) | | °C | TGA | As received | 315 |
| | Time to Delam ( T288 ) | Without Cu | Min | IPC TM-650 2.4.24.1 | As received | 5 |
| | | With Cu | Min | IPC TM-650 2.4.24.1 | As received | 1 |
| | CTE : $\alpha 1$ | X - axis | ppm / C | IPC TM-650 2.4.24 | < Tg | 11 – 13 |
| | | Y - axis | ppm / C | IPC TM-650 2.4.24 | < Tg | 13 – 15 |
| | | Z - axis | ppm / C | IPC TM-650 2.4.24 | < Tg | 65 |
| | CTE : $\alpha 2$ | Z - axis | ppm / C | IPC TM-650 2.4.24 | > Tg | 270 |

## Via fatigue calculator

| Curve | Cycles to 63% failure | Cycles to 50% failure | Cycles to 5% failure | Cycles to 1% failure |
|---|---|---|---|---|
| **Curve 1** | 963 | 920 | 665 | 542 |
| **Curve 2** | 1184 | 1132 | 817 | 667 |



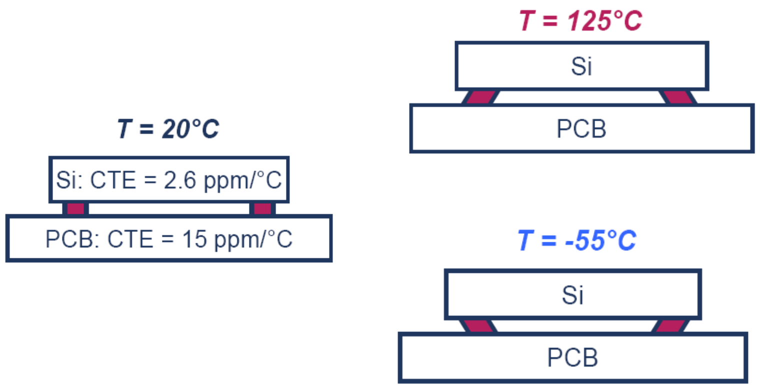
**Conclusion: The via fatigue calculator would perfectly have predicted this failure risk**

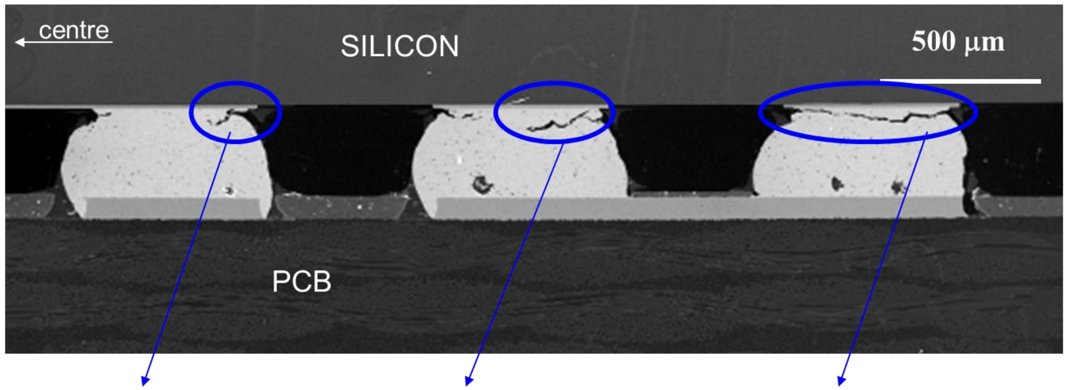
# SOLDER FATIGUE MODEL

# 2. SOLDER FATIGUE OF ASSEMBLED COMPONENTS

## DAMAGE INDUCED BY DEFORMATION MISMATCH BETWEEN COMPONENT & PCB

**Damage Mechanism**



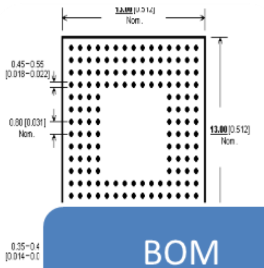


Micro-crack initation

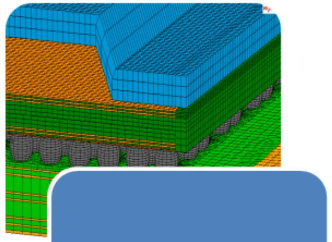
Crack propagation

Fracture

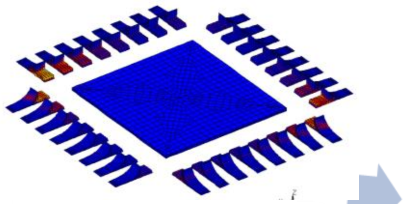
**Quantification**



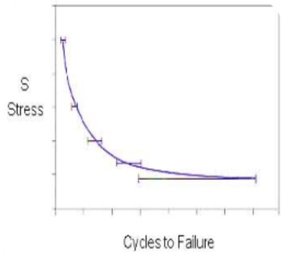
BOM
+
Mission profile



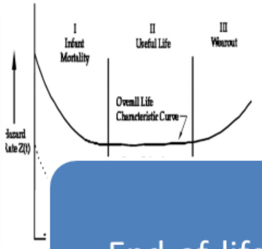
Modelling / Quantification / Simulation



Cyclic strain in solder joints



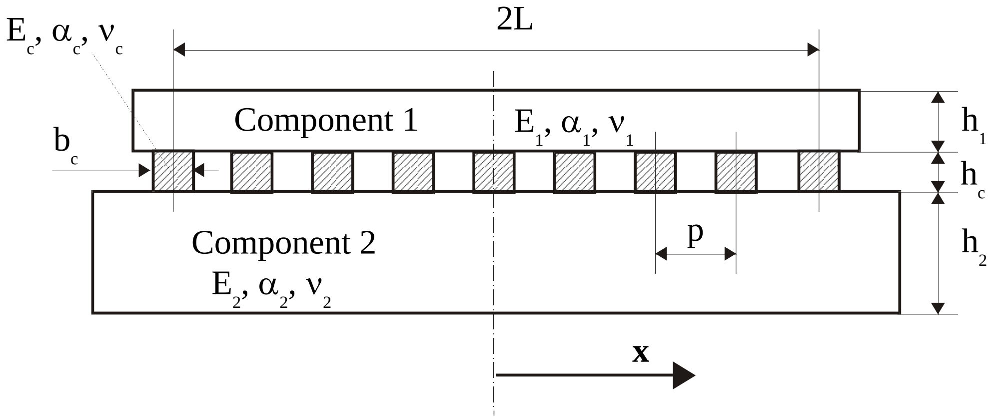
Life time model



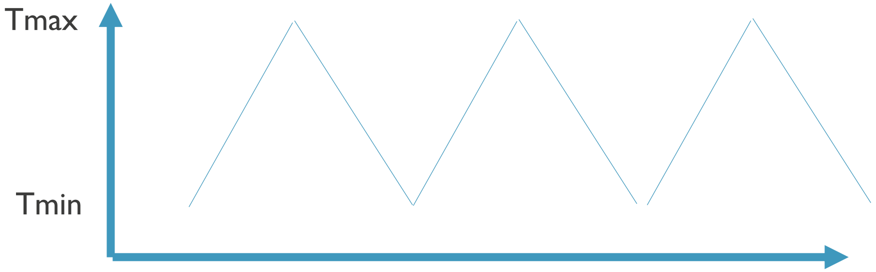
End-of-life prediction (MTTF)

# SOLDER FATIGUE CALCULATOR BASED ON ANALYTICAL EQUATIONS

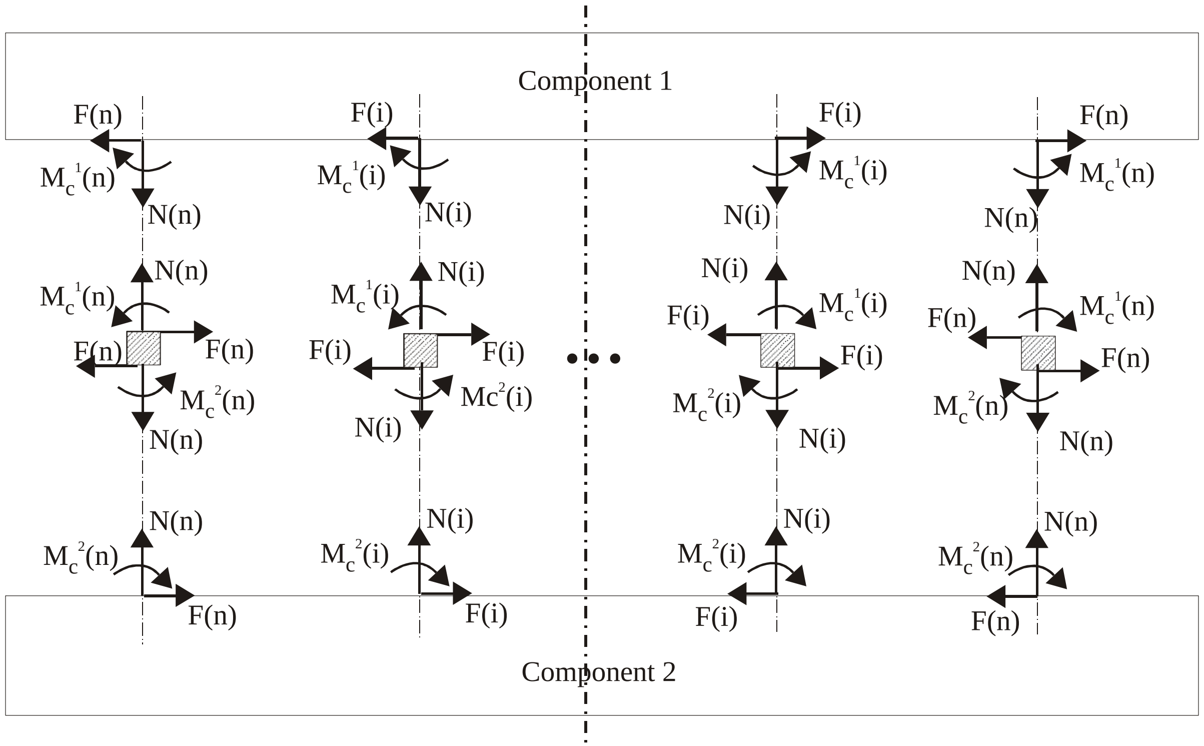
## Geometry



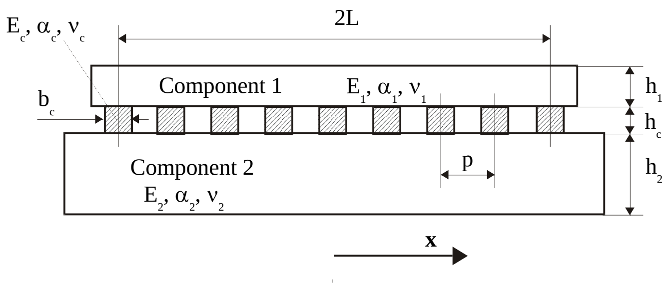
## Loading



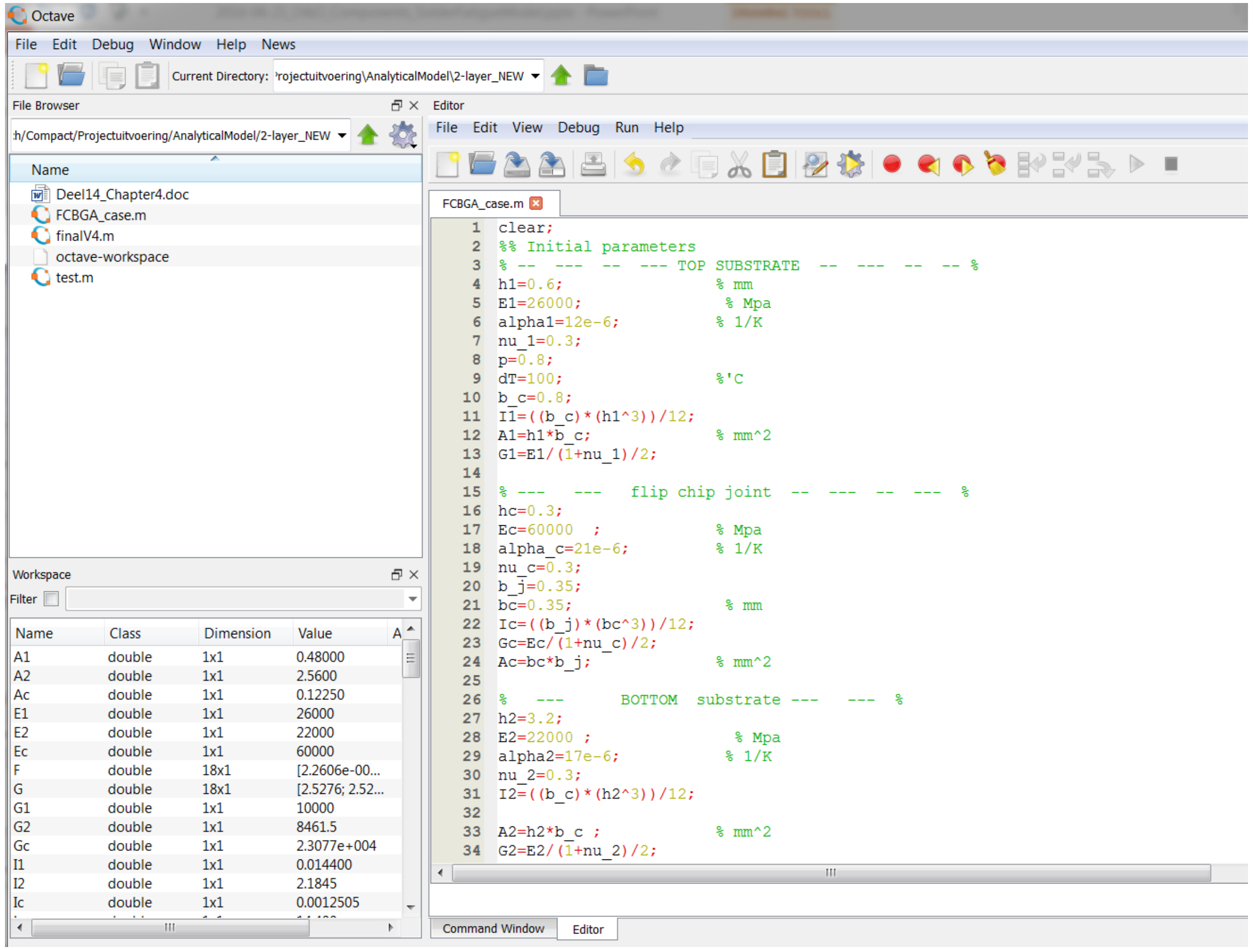
## Forces & Moments acting on interconnects



# SOLDER FATIGUE CALCULATOR BASED ON ANALYTICAL EQUATIONS



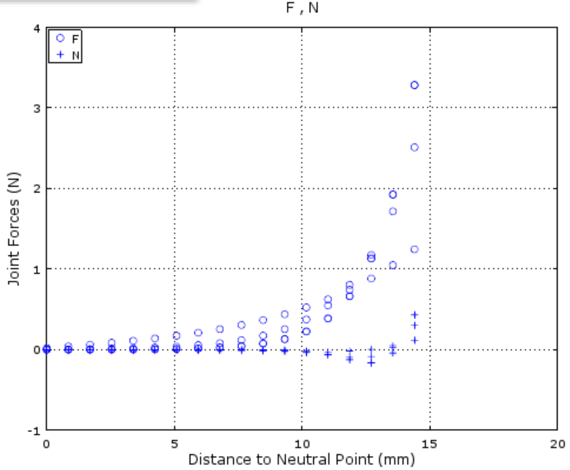
**Implementation in Matlab**

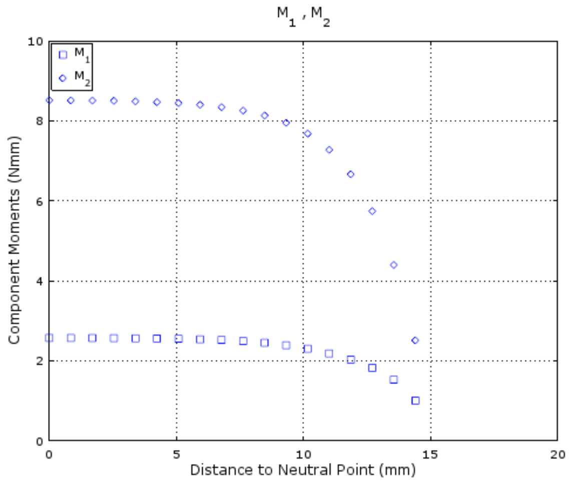


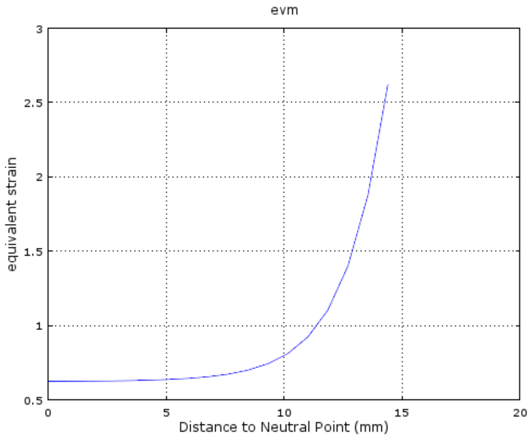
```
clear;
%% Initial parameters
% --  ---  --  --- TOP SUBSTRATE  --  ---  --  -- %
h1=0.6;                        % mm
E1=26000;                       % Mpa
alpha1=12e-6;                  % 1/K
nu_1=0.3;
p=0.8;
dT=100;                        %'C
b_c=0.8;
I1=((b_c)*(h1^3))/12;
A1=h1*b_c;                     % mm^2
G1=E1/(1+nu_1)/2;

% ---   ---   flip chip joint  --  ---  --  ---  %
hc=0.3;
Ec=60000  ;                    % Mpa
alpha_c=21e-6;                 % 1/K
nu_c=0.3;
b_j=0.35;
bc=0.35;                        % mm
Ic=((b_j)*(bc^3))/12;
Gc=Ec/(1+nu_c)/2;
Ac=bc*b_j;                     % mm^2

%   ---      BOTTOM  substrate ---   ---  %
h2=3.2;
E2=22000 ;                       % Mpa
alpha2=17e-6;                   % 1/K
nu_2=0.3;
I2=((b_c)*(h2^3))/12;

A2=h2*b_c ;                    % mm^2
G2=E2/(1+nu_2)/2;
```

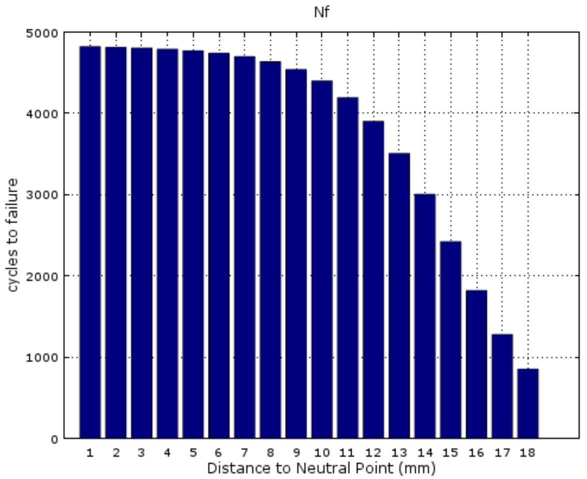
| Name | Class | Dimension | Value |
|---|---|---|---|
| A1 | double | 1x1 | 0.48000 |
| A2 | double | 1x1 | 2.5600 |
| Ac | double | 1x1 | 0.12250 |
| E1 | double | 1x1 | 26000 |
| E2 | double | 1x1 | 22000 |
| Ec | double | 1x1 | 60000 |
| F | double | 18x1 | [2.2606e-00... |
| G | double | 18x1 | [2.5276; 2.52... |
| G1 | double | 1x1 | 10000 |
| G2 | double | 1x1 | 8461.5 |
| Gc | double | 1x1 | 2.3077e+004 |
| I1 | double | 1x1 | 0.014400 |
| I2 | double | 1x1 | 2.1845 |
| Ic | double | 1x1 | 0.0012505 |

**OUTPUT**



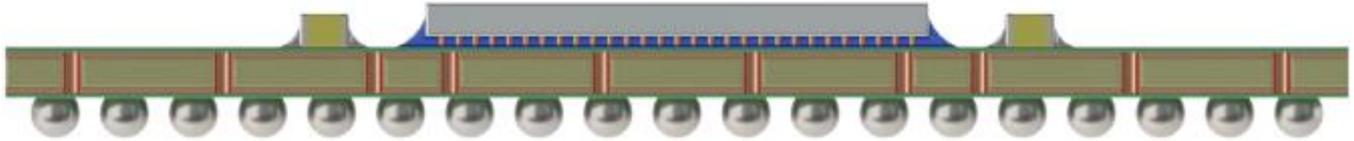


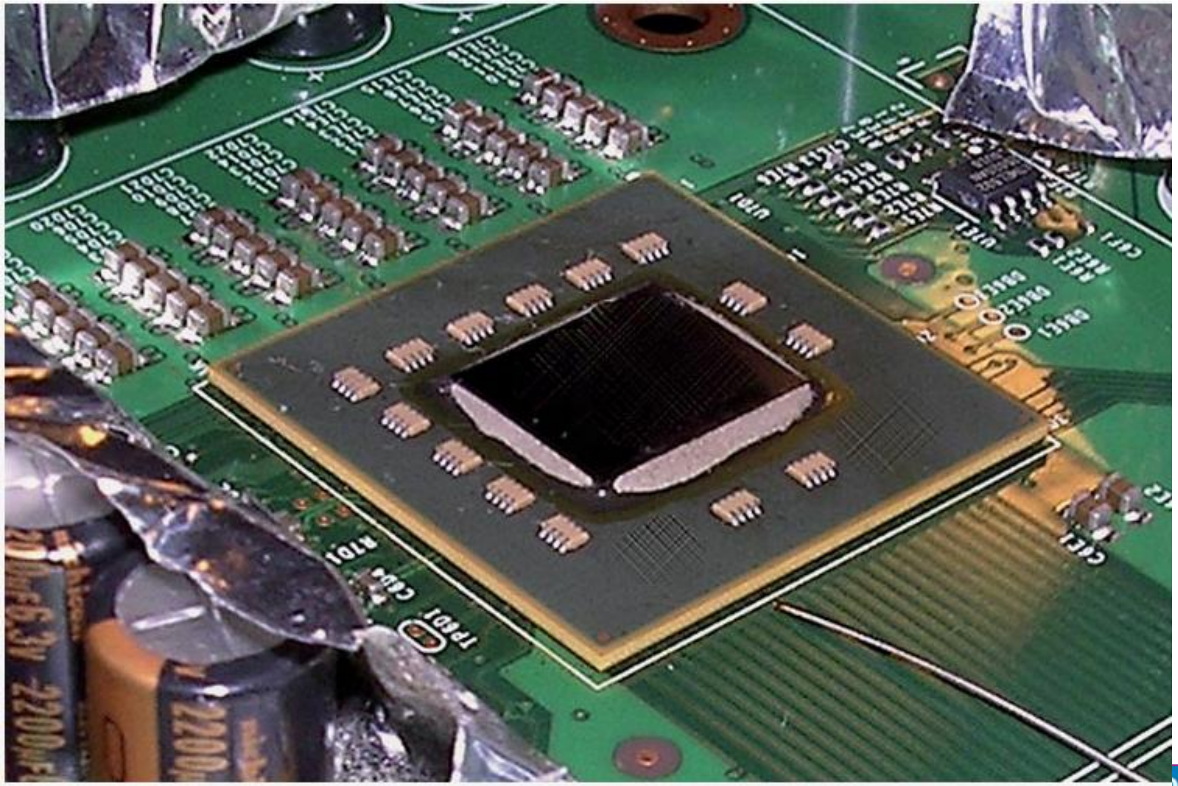




# EXAMPLE CASE: FLIP CHIP BGA

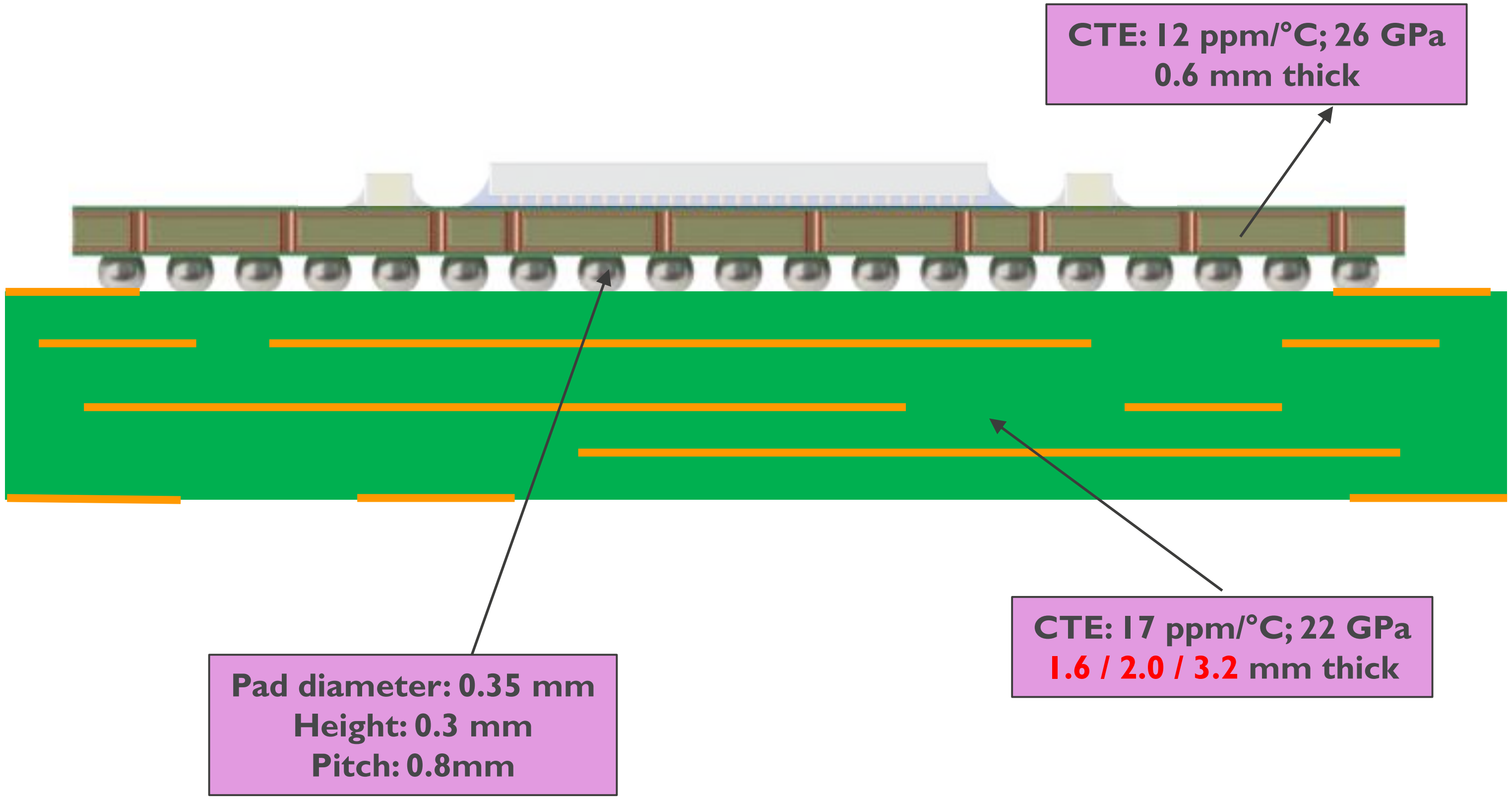
- Body size: 29x29 mm
- Pitch: 0.8 mm
- #I/O's: 1225 (35x35)





# EXAMPLE CASE: FLIP CHIP BGA

- Loading: Thermal Cycling between 0°C to +100°C



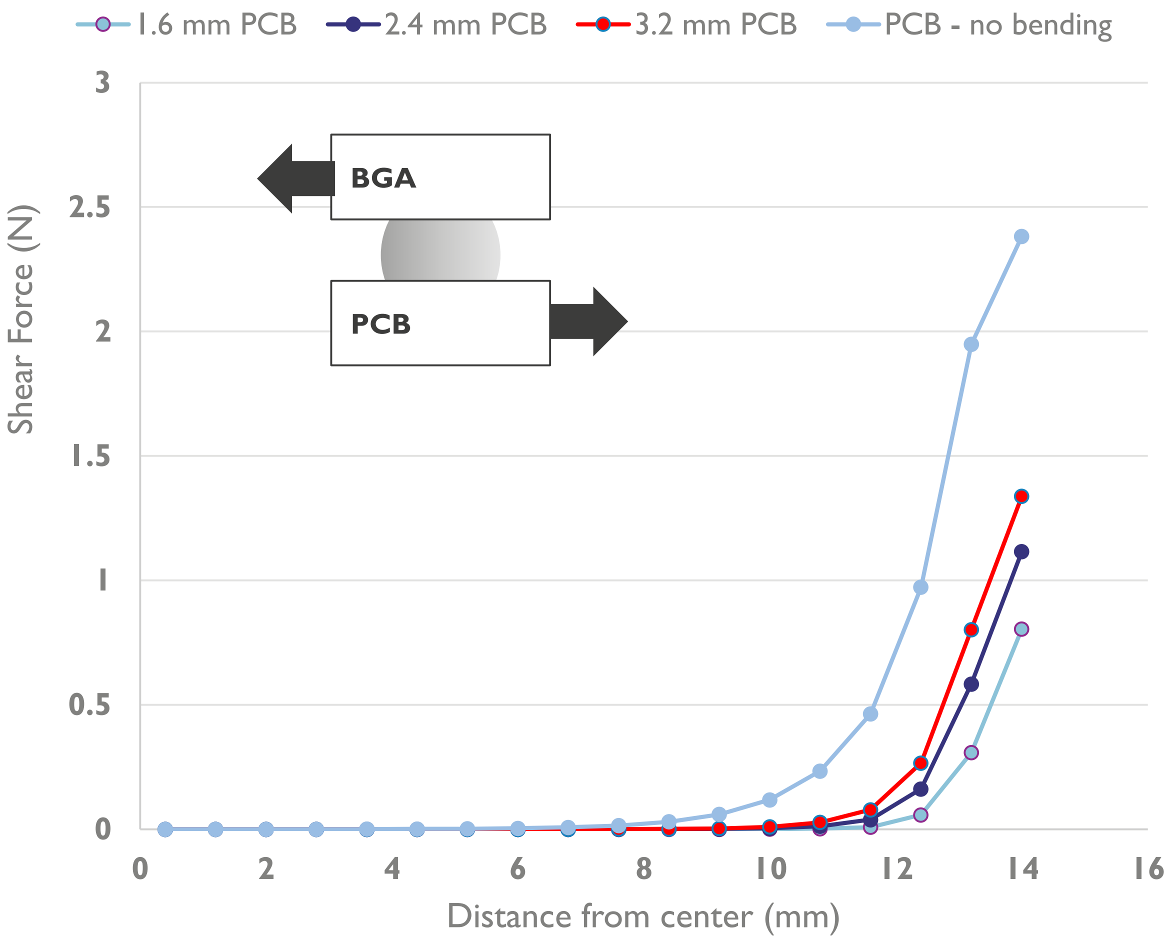
CTE: 12 ppm/°C; 26 GPa
0.6 mm thick

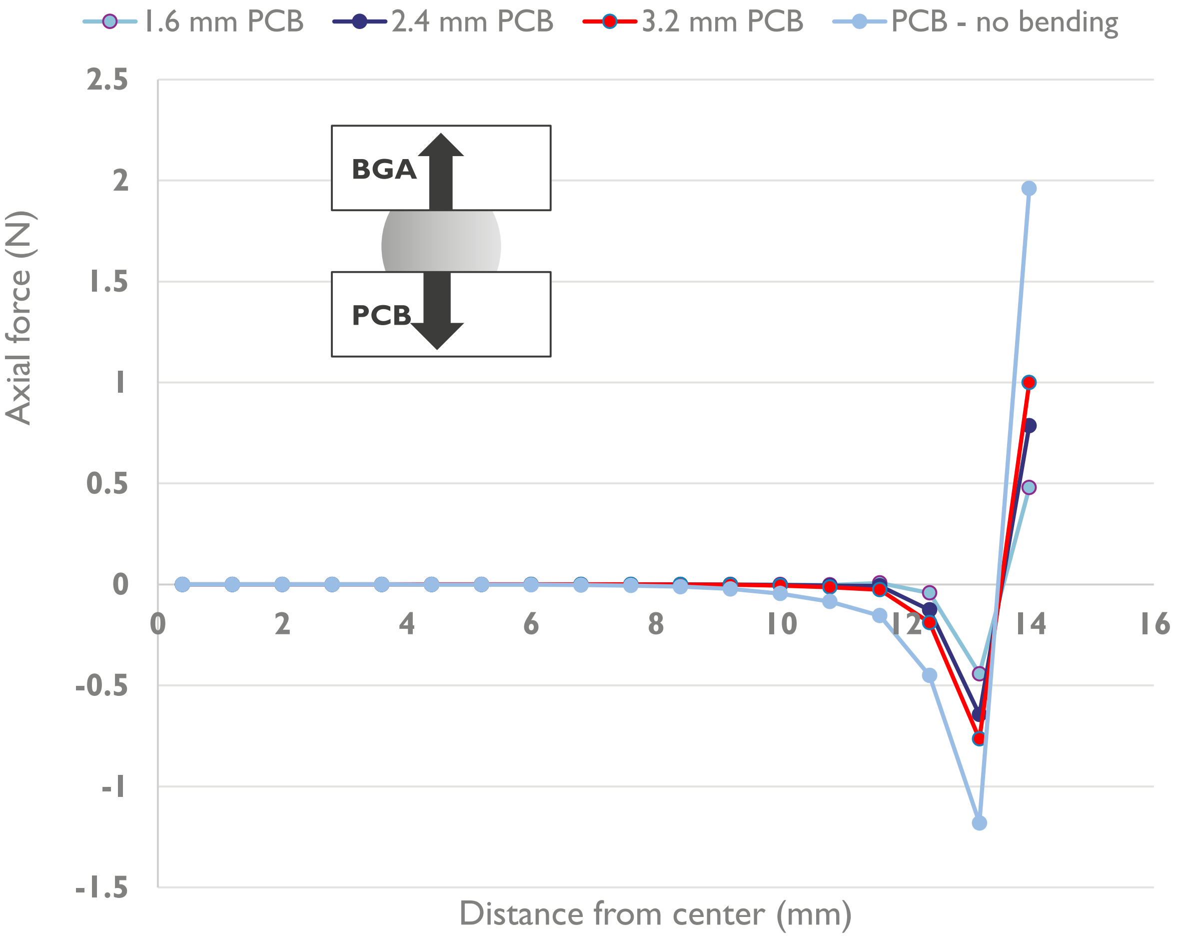
Pad diameter: 0.35 mm
Height: 0.3 mm
Pitch: 0.8mm

CTE: 17 ppm/°C; 22 GPa
1.6 / 2.0 / 3.2 mm thick

# RESULTS

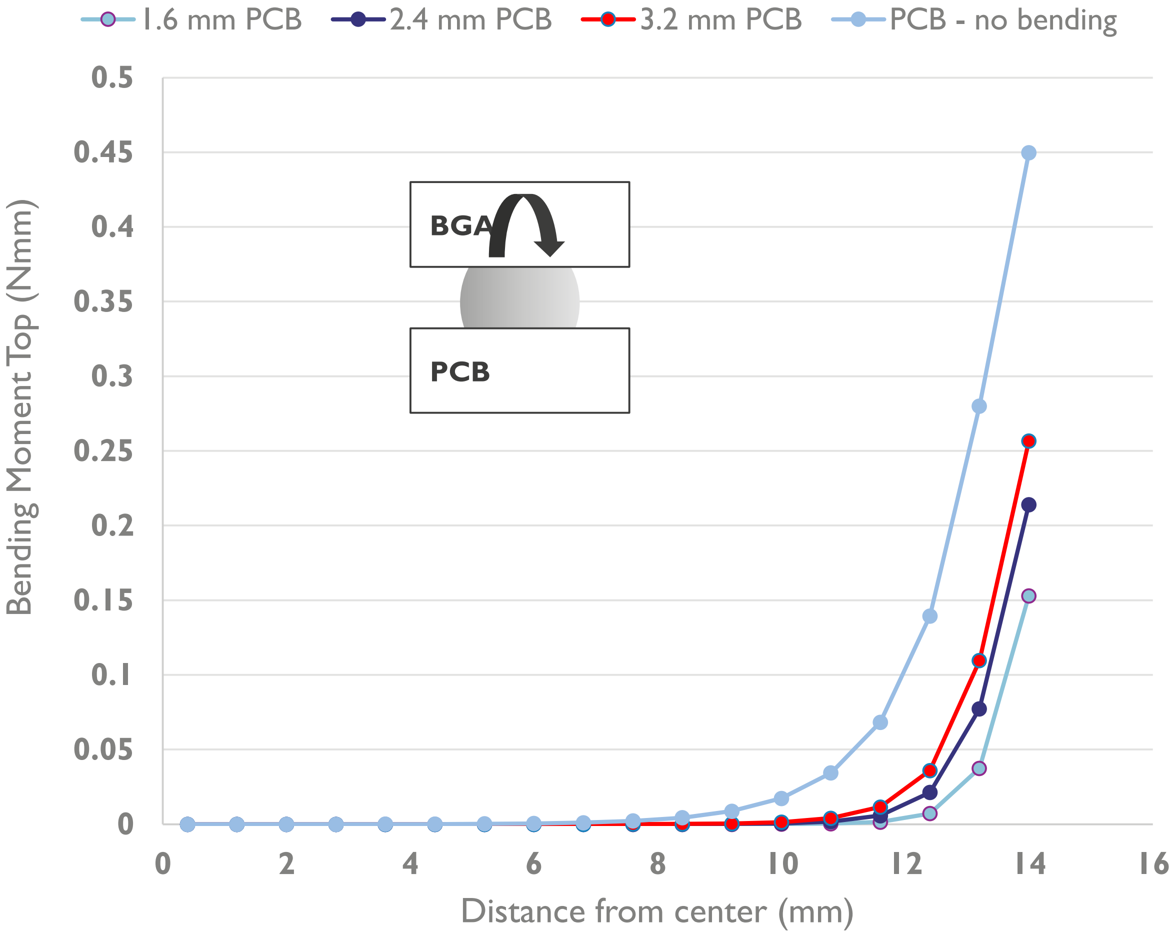
## FORCES ACTING ON SOLDER JOINTS (INCREASE FROM 0°C → 100°C)

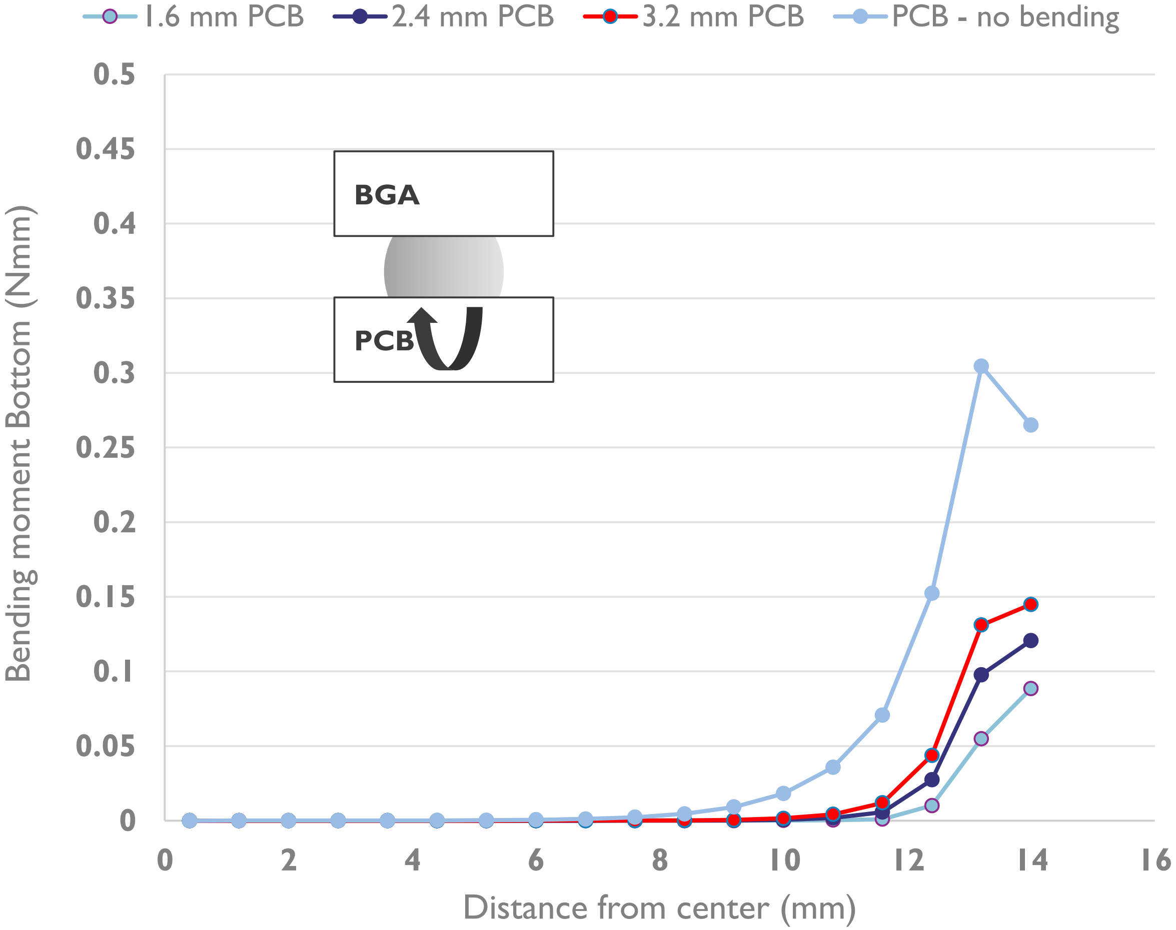




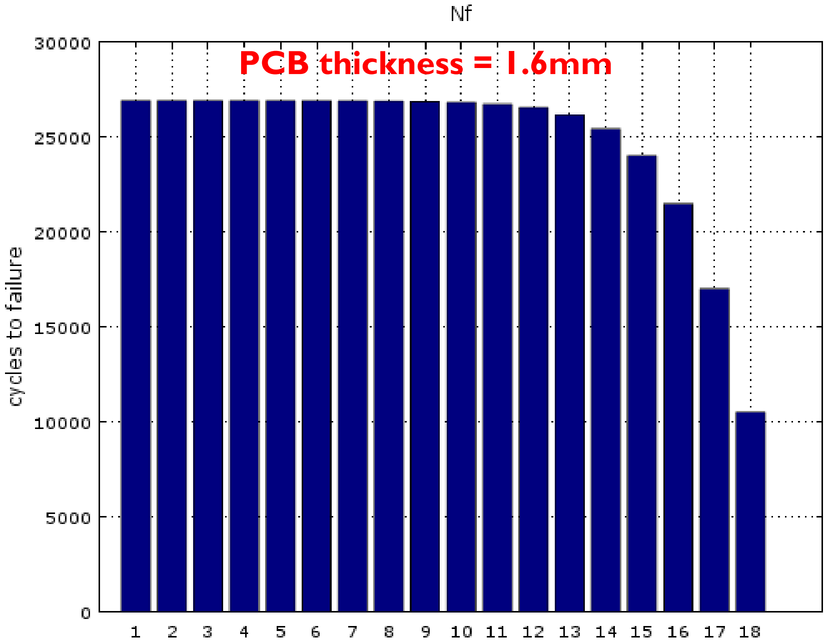
# RESULTS

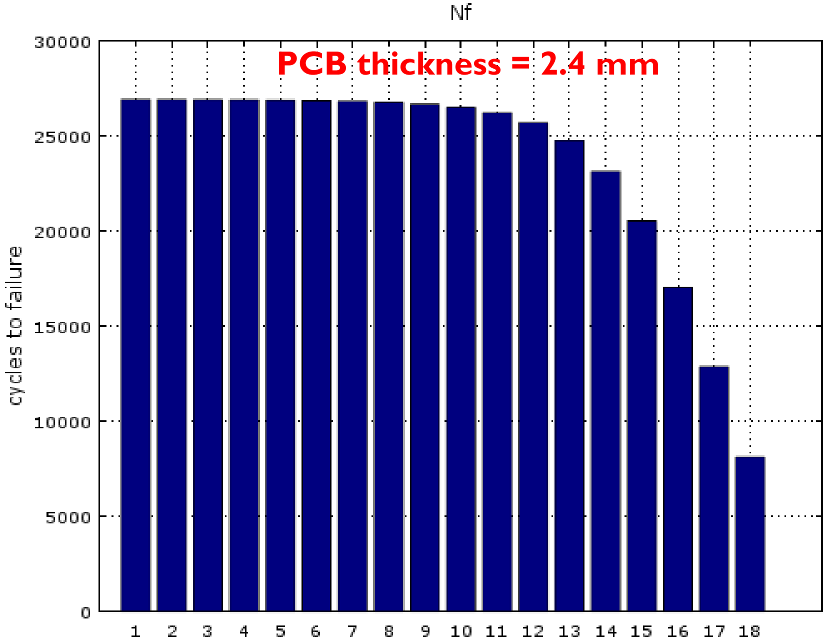
## BENDING MOMENTS ACTING ON SOLDER JOINTS (INCREASE FROM 0°C → 100°C)



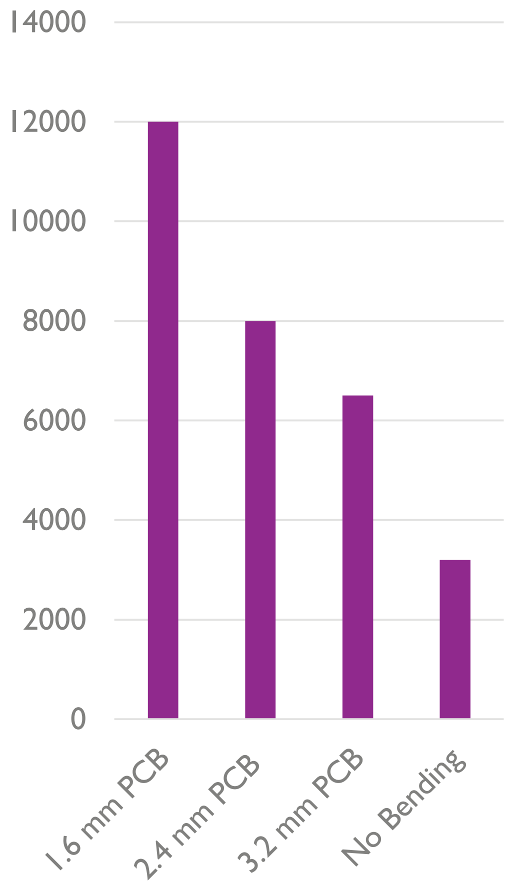


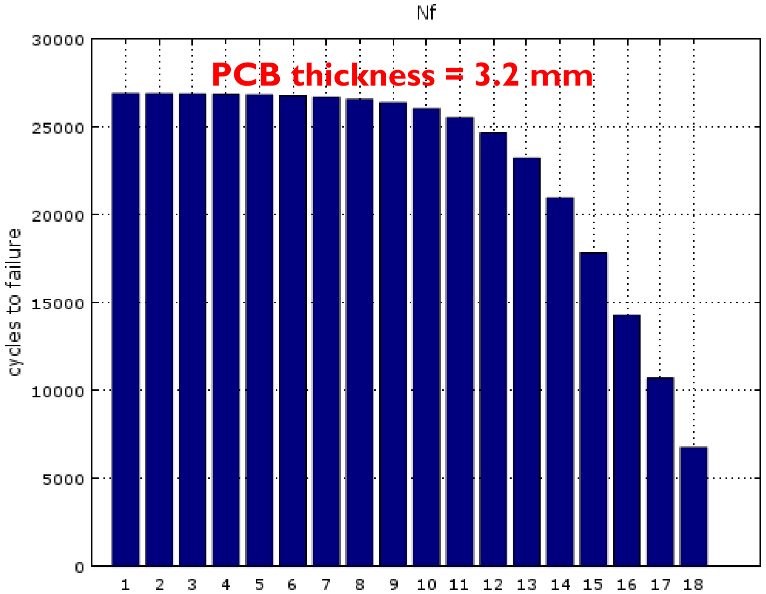
# LIFE TIME PREDICTIONS

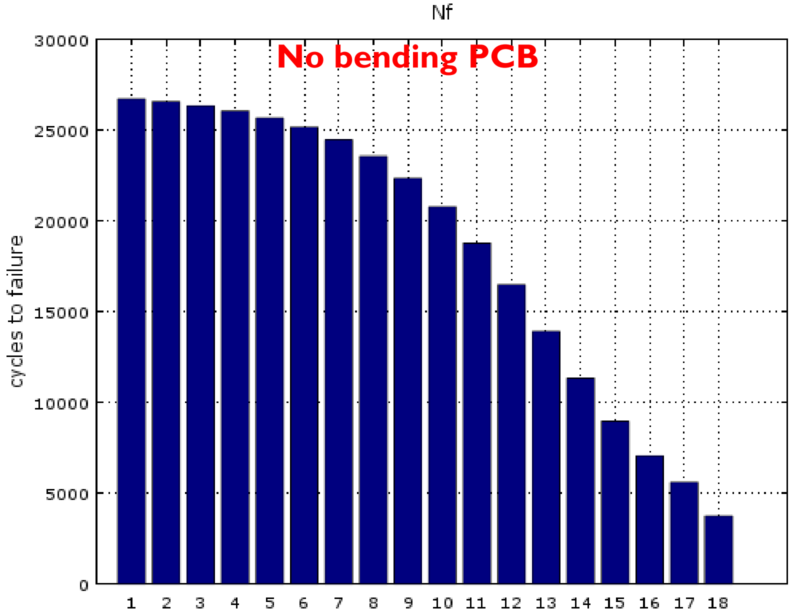




Life time in cycles to failure



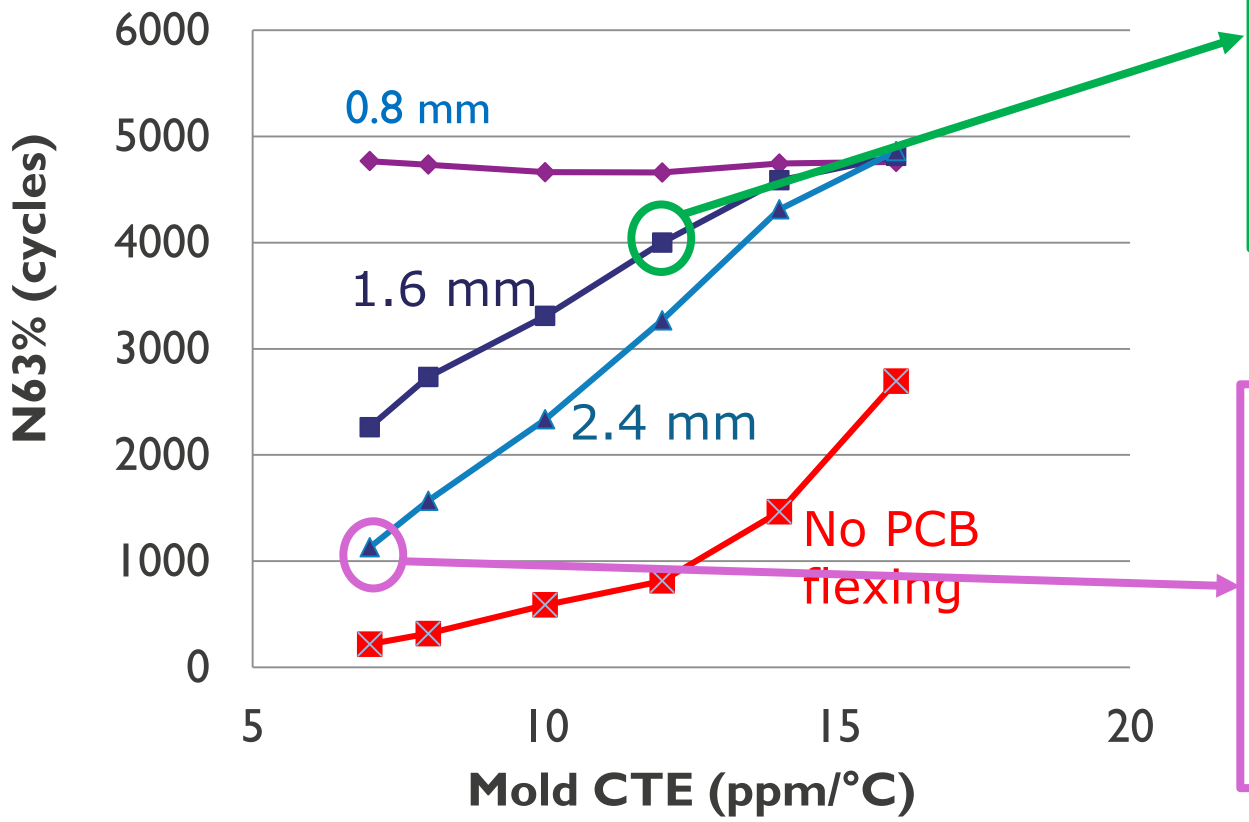




# RELEVANCE OF (NON)-FLEXIBILITY OF PCB'S

## RESULTS BASED ON FEM SIMULATIONS

*Example: PBGA 27x27 area array 1.27mm pitch*

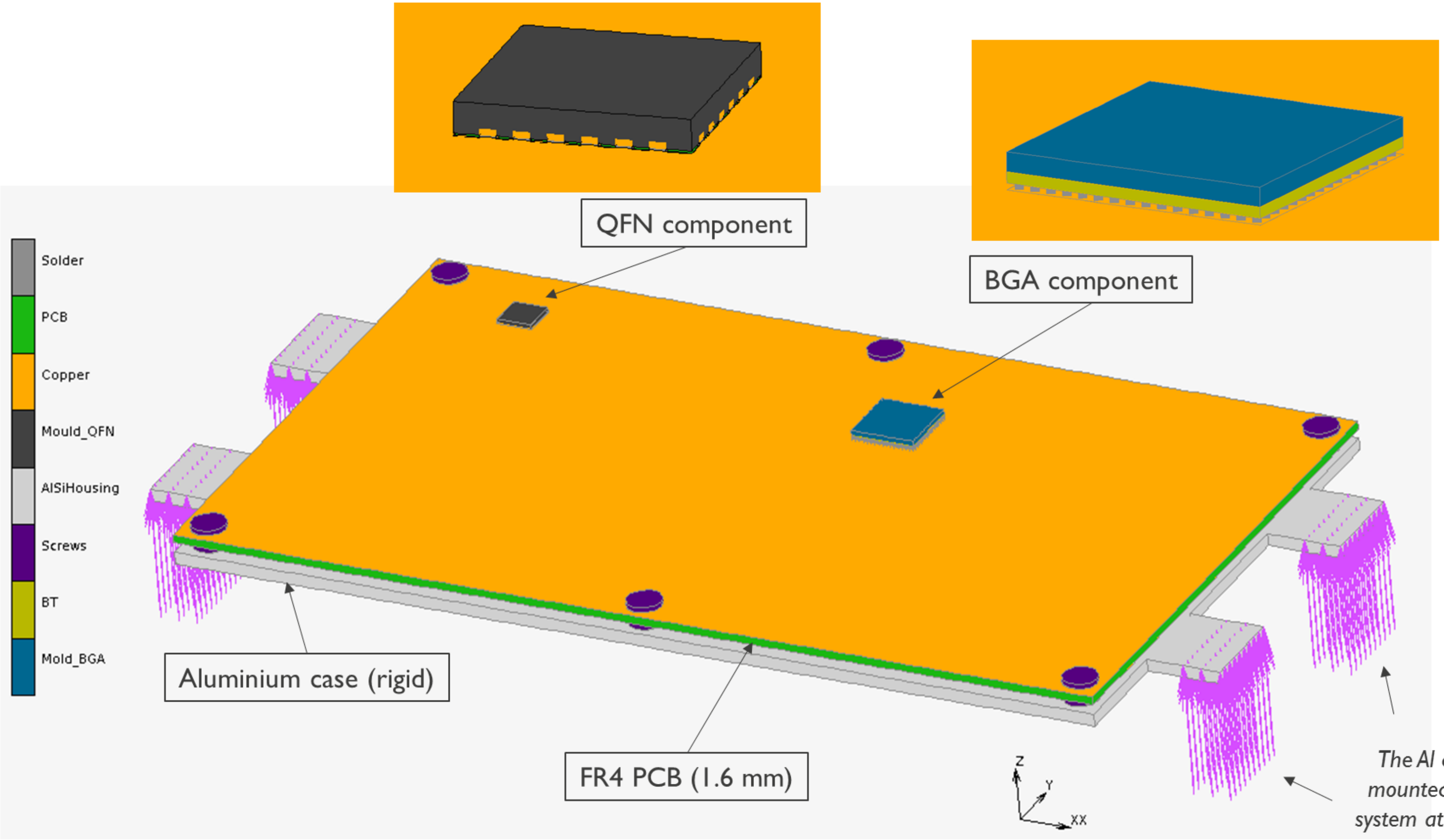


- PBGA supplier guarantees "minimum 2000 cycles with zero failures"
- Tests were performed for 1.6 mm **test** board

- PBGA supplier changed mould compound without notification
- PBGA is assembled to rigid 2.4 mm **application** board
- Failures after 1000 cycles

# VIRTUAL PROTOTYPING OF ELECTRONIC SYSTEMS

## THERMAL CYCLING RELIABILITY



QFN component

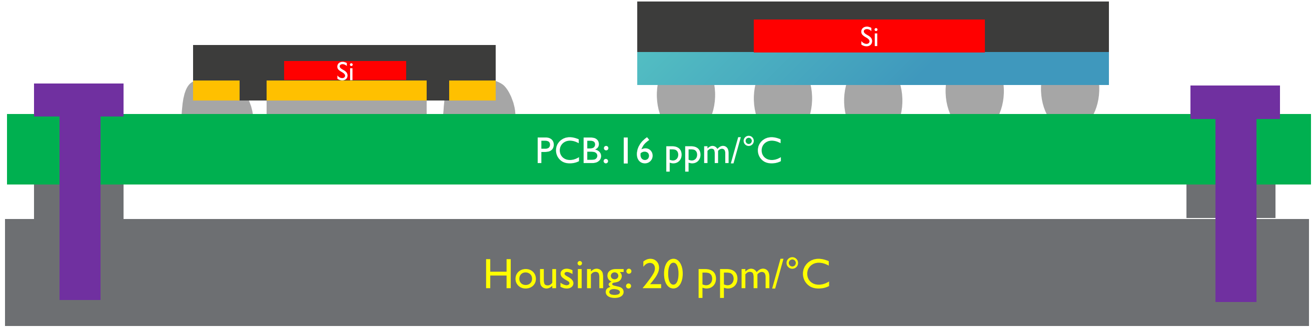
BGA component

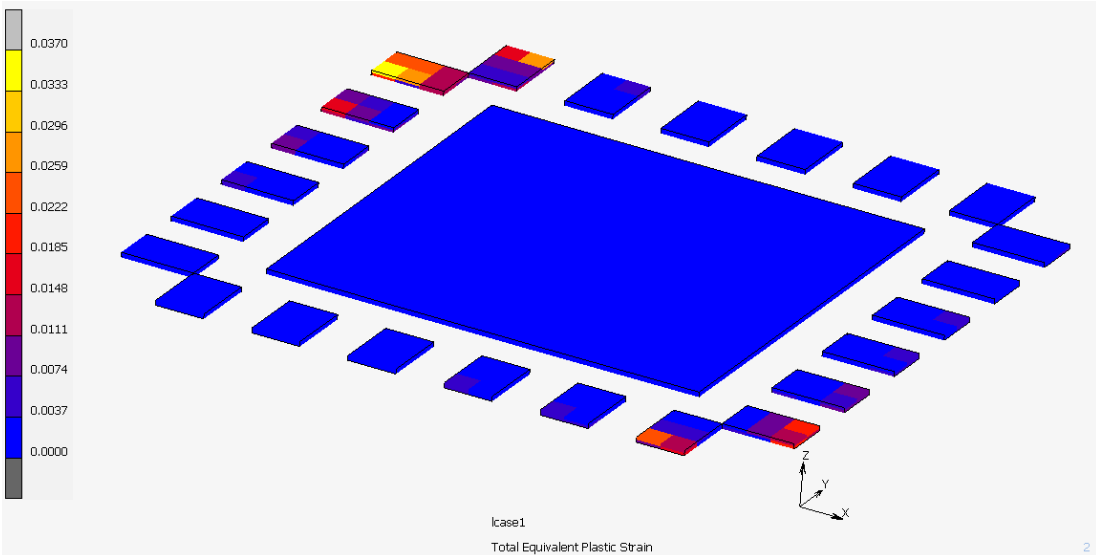
Aluminium case (rigid)

FR4 PCB (1.6 mm)

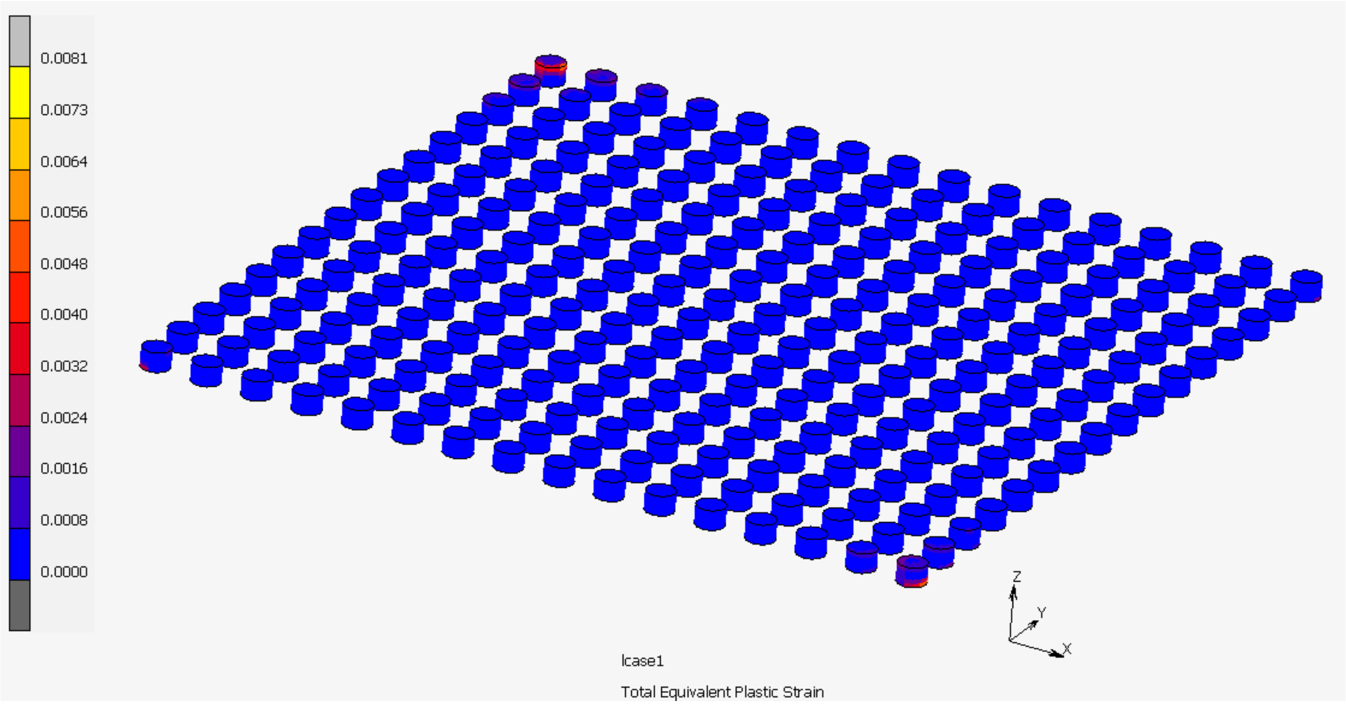
*The Al case is mounted to the system at 4 points*

# THERMAL CYCLING OF PRODUCT = APPLICATION BOARD MOUNTED IN HOUSING





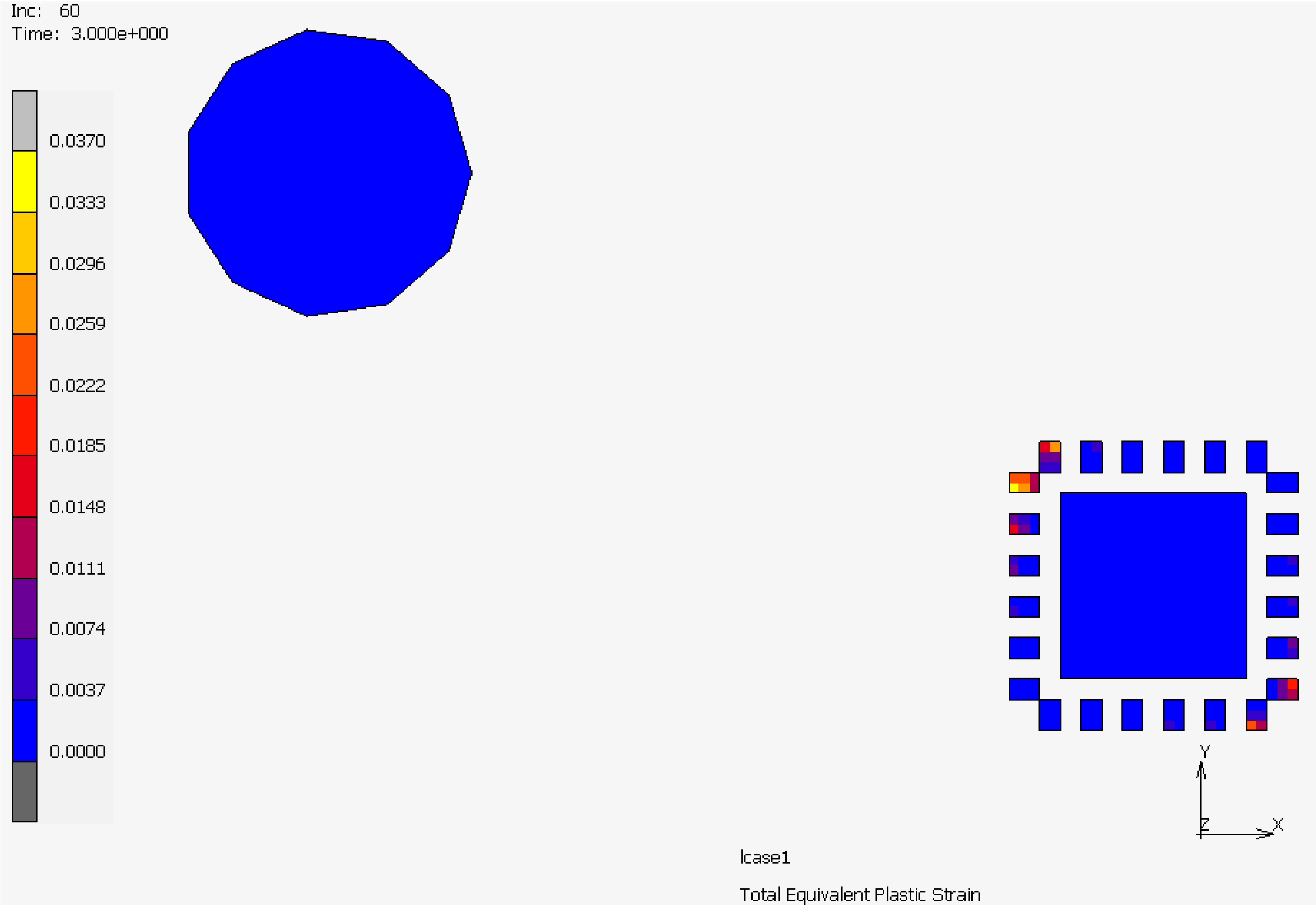
N63% = 1140 cycles to failure



N63% = 3600 cycles to failure

# THERMAL CYCLING

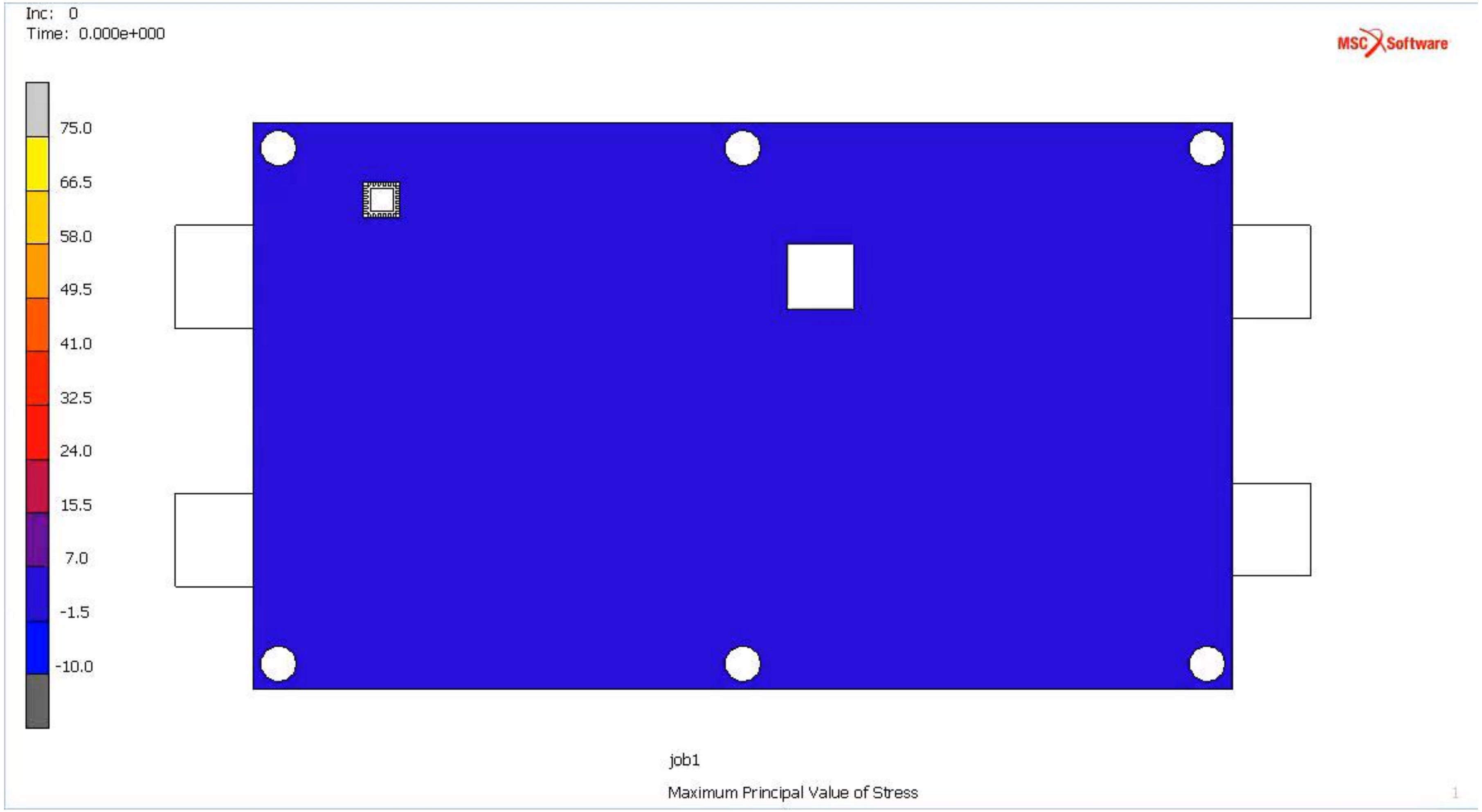
## INELASTIC STRAIN PER CYCLE IN QFN SOLDER JOINTS



Strain per cycle: 3.7%

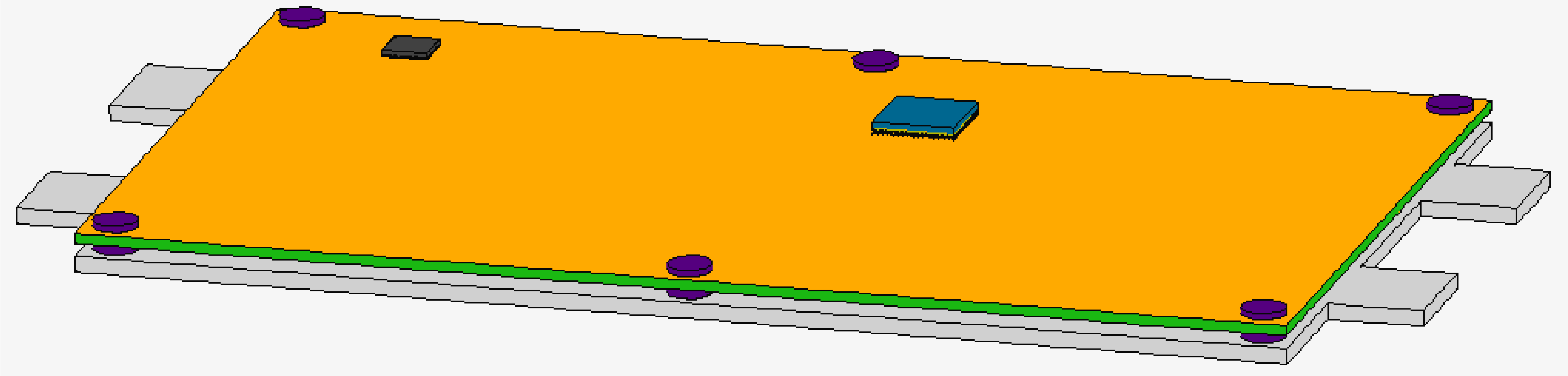
N63% = 1140 cycles

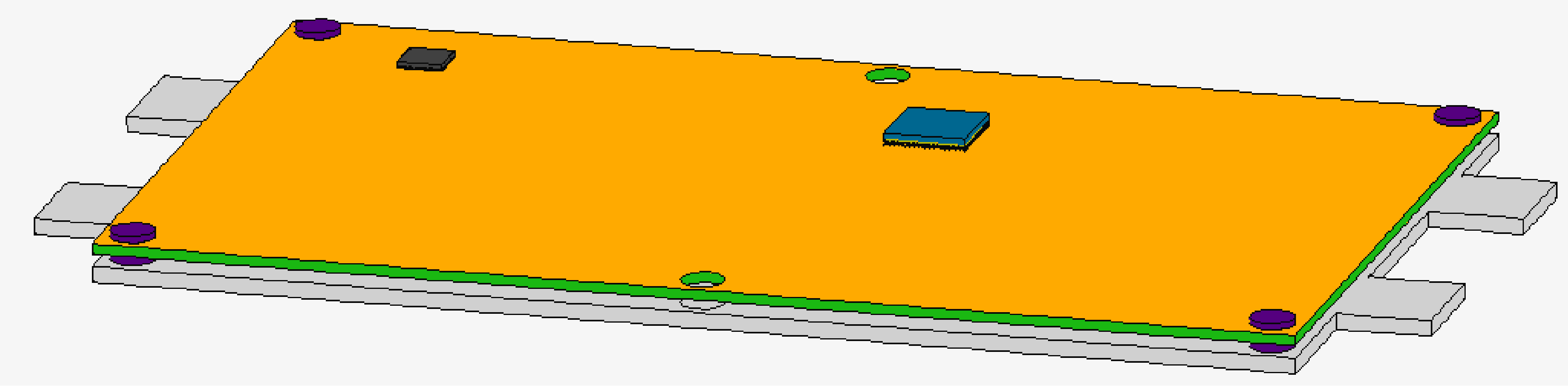
✗

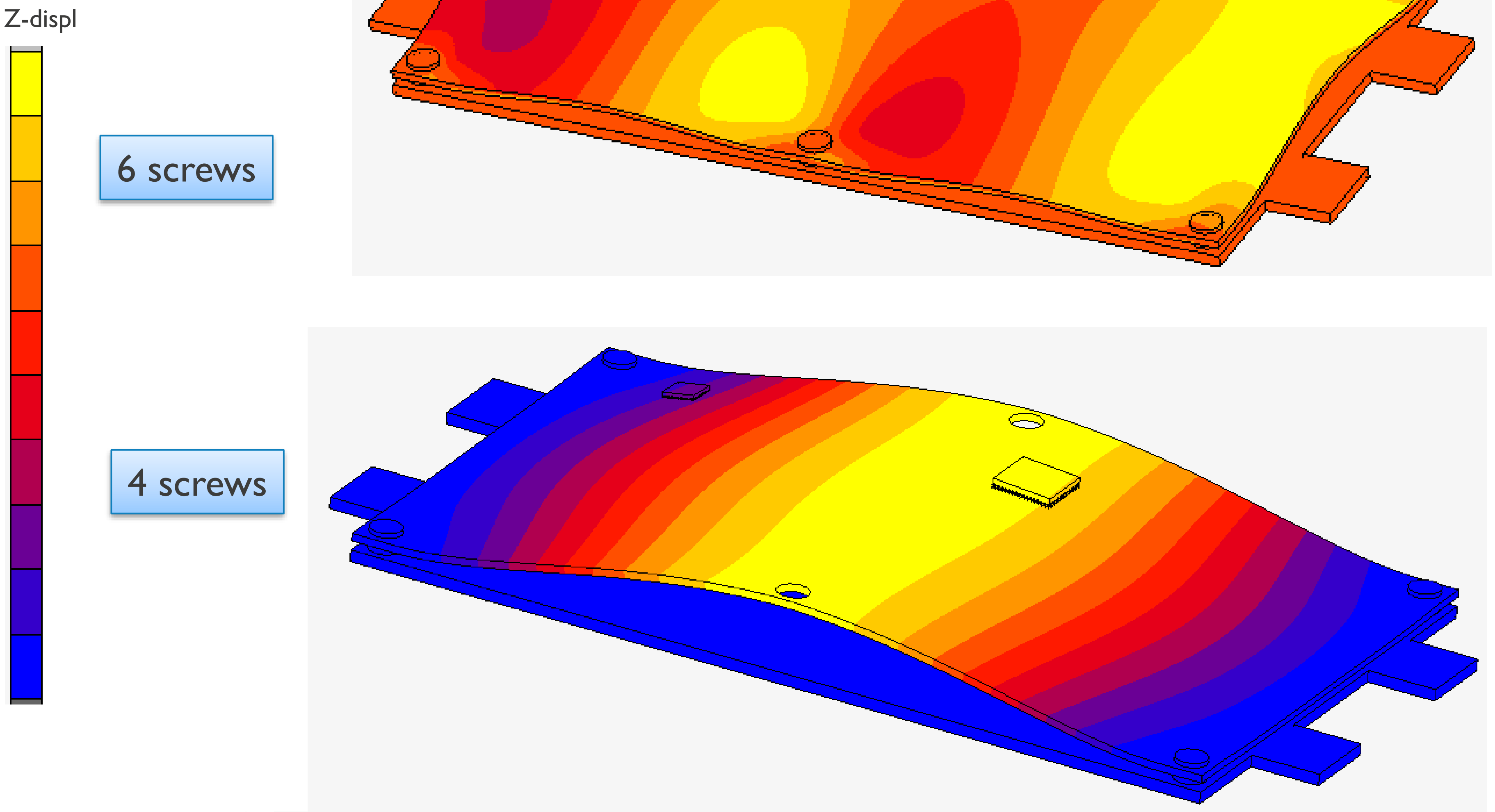


Inc: 0
Time: 0.000e+000
MSC Software
75.0
66.5
58.0
49.5
41.0
32.5
24.0
15.5
7.0
-1.5
-10.0
job1
Maximum Principal Value of Stress
1

# HARMONIC ANALYSIS







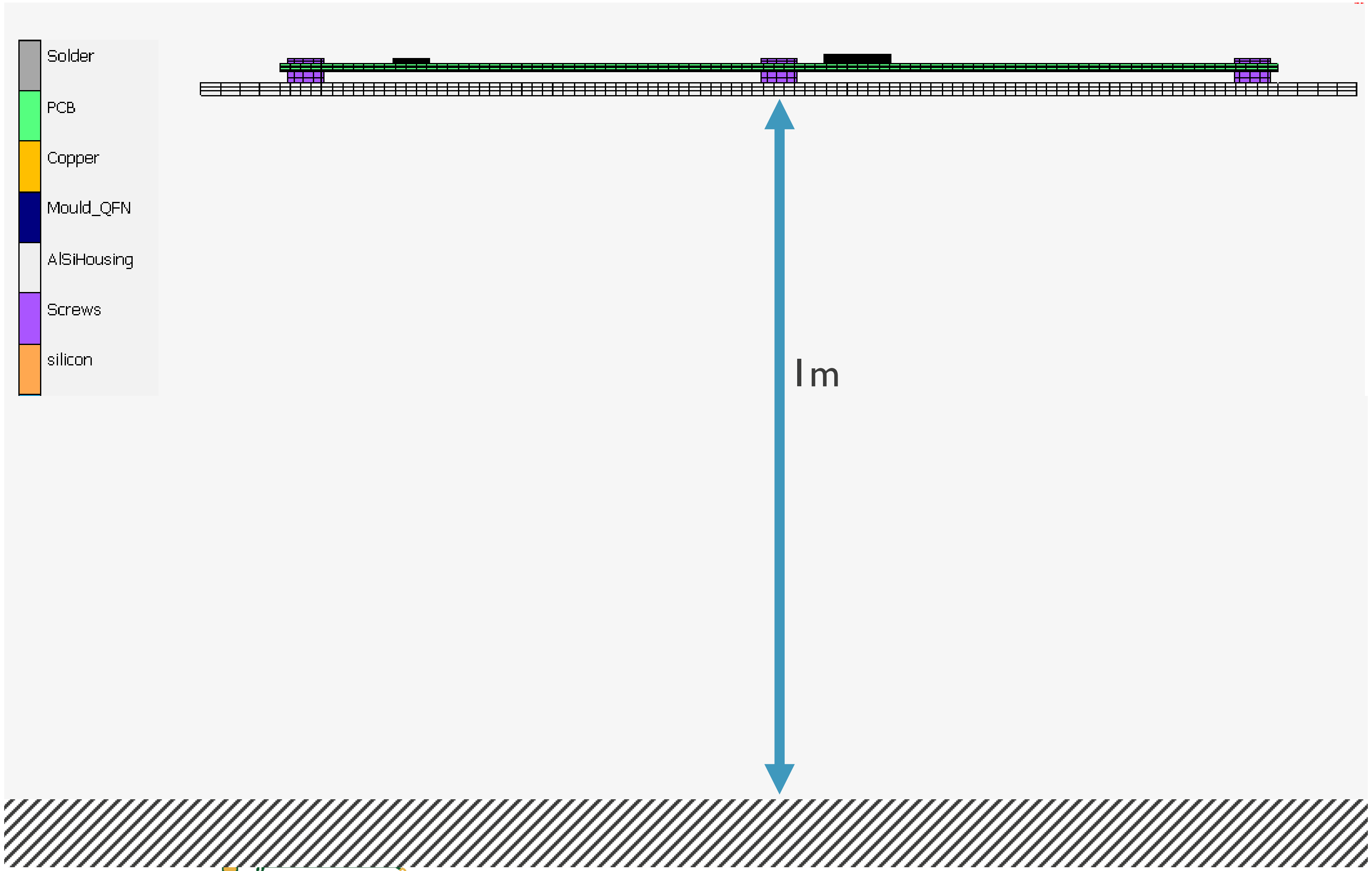
6 screws

417 Hz ✓

4 screws

142 Hz ✗

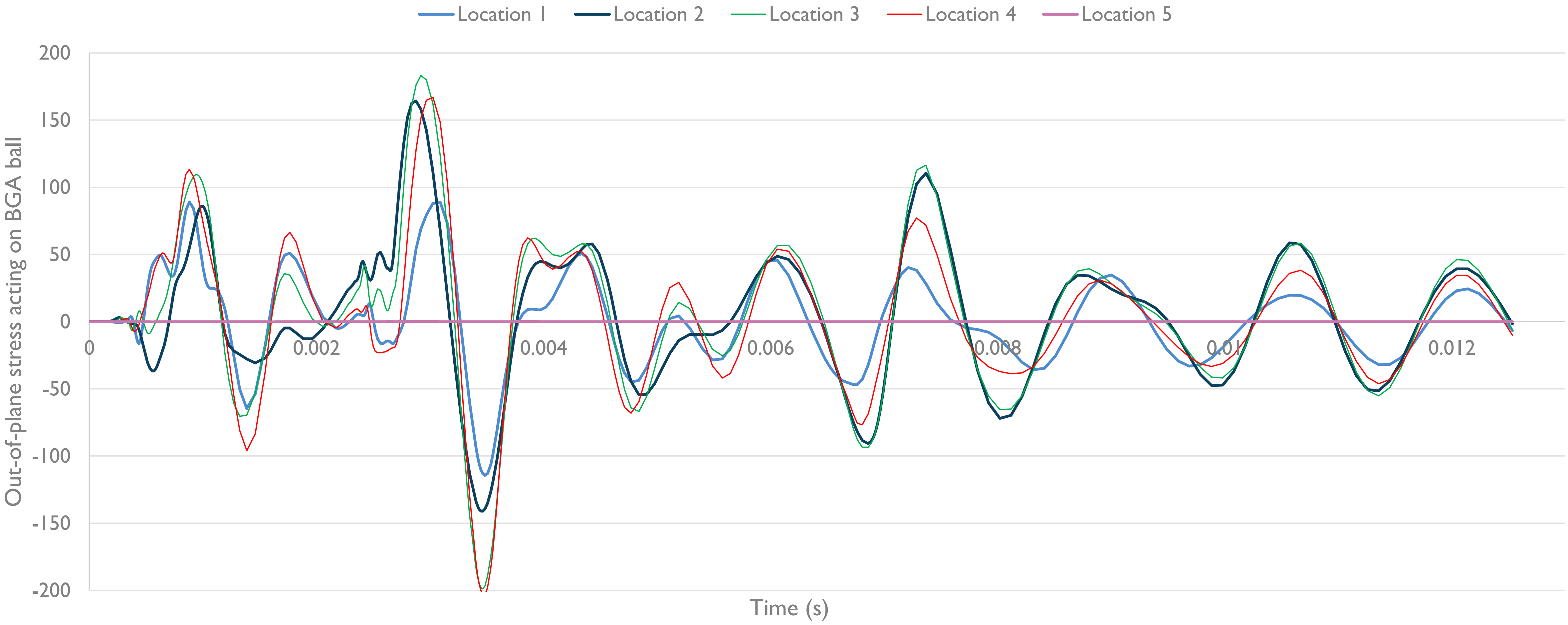
# REPRESENTATION OF 1M DROP TEST



Sample has a velocity of **4.4 m/s** when it touches the ground

# RESULTS

## STRESS IN THE **SOLDER JOINTS** IN THE FOUR CORNER LOCATIONS + CENTER OF THE BGA



# DETERMINING THE SAFETY MARGIN A FOR SOLDER FATIGUE

## RELIABILITY DATA FROM ACCELERATED THERMAL CYCLING TESTING

Three parameter Weibull

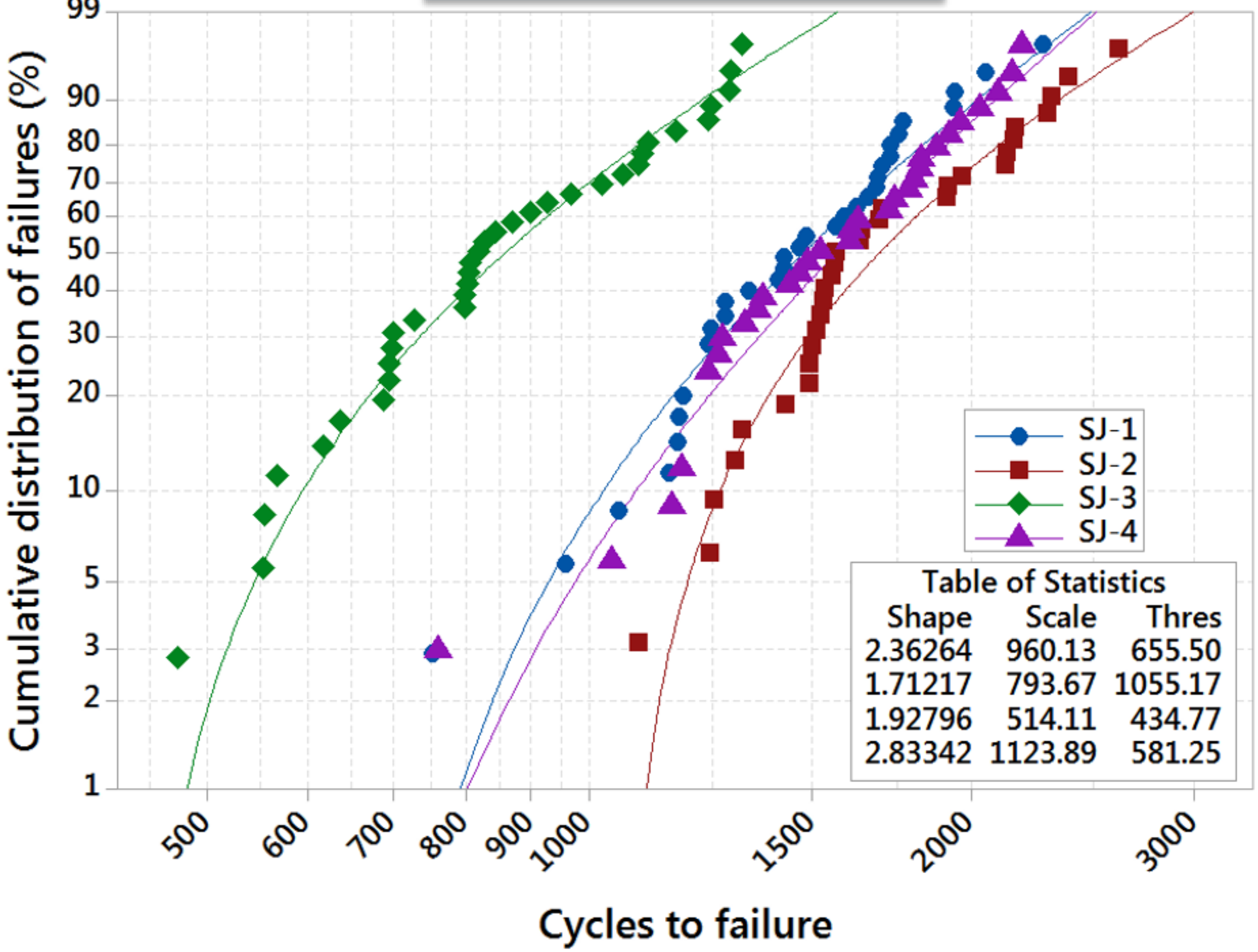


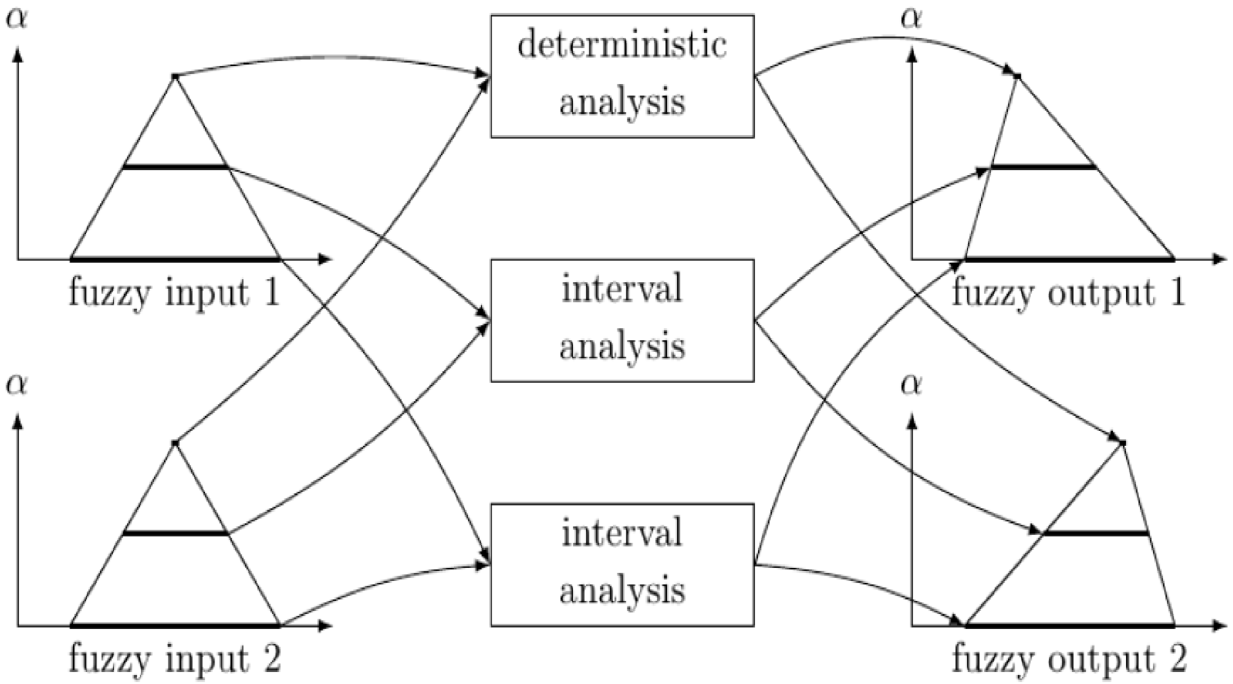
Table of Statistics

| Shape | Scale | Thres |
|---|---|---|
| 2.36264 | 960.13 | 655.50 |
| 1.71217 | 793.67 | 1055.17 |
| 1.92796 | 514.11 | 434.77 |
| 2.83342 | 1123.89 | 581.25 |

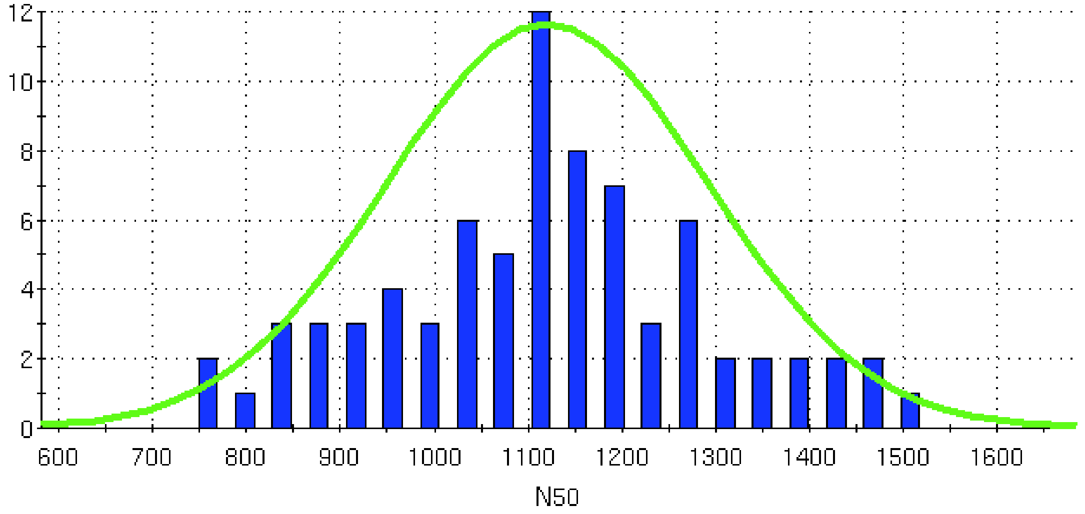
| # | Failure Free Time | $N_{63\%}$ | A |
|---|---|---|---|
| SJ-1 | 656 | 1616 | 2.5 |
| SJ-2 | 1055 | 1849 | 1.8 |
| SJ-3 | 435 | 949 | 2.2 |
| SJ-4 | 581 | 1705 | 2.9 |

Safety margin A = **3**

# VIRTUAL PROTOTYPING WITH UNCERTAINTIES

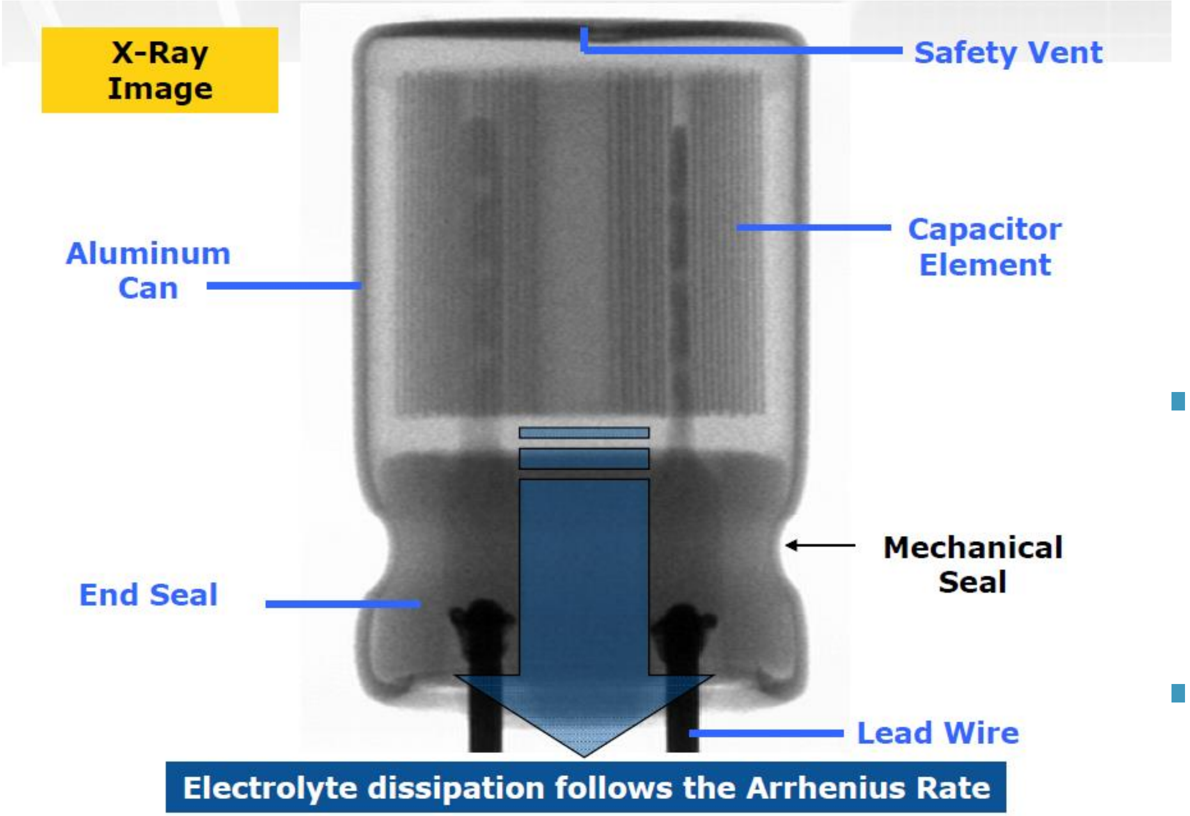


| Parameter | Nominal value | Tolerance (= $3\sigma$) |
|---|---|---|
| Substrate pad diameter | 270 µm | ± 25 µm |
| Chip pad diameter | 280 µm | ± 25 µm |
| Solder volume | 0.01745 mm$^3$ | ± 0.002 mm$^3$ |
| Chip thickness | 0.650 | ± 0.050 |
| Elastic Modulus of PCB | 25 GPa | ± 2.5 GPa |
| CTE of PCB | 16e-6 1/°C | ± 2e-6 1/°C |



# AL CAPACITOR DEGRADATION MODEL

# 3. AL CAPACITOR DEGRADATION

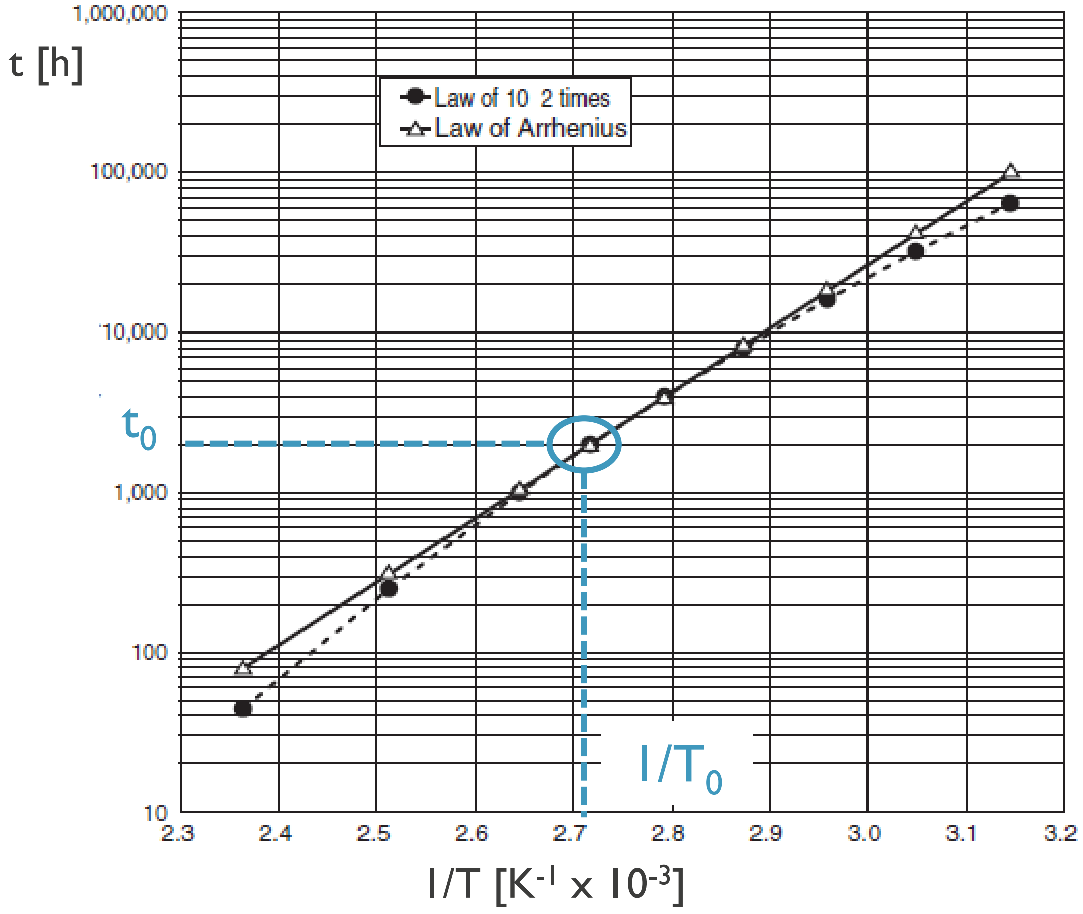


Source: NIC Comp. Technical Note
"Selection (and precautions for use)of Aluminum Electrolytic Capacitors in LED Lighting Applications"

- When capacitors are used in power supplies and signal filters, degradation in the capacitors increases the impedance path for the AC current and decrease in capacitance introduces ripple voltage on top of the desired DC voltage.
- Continued degradation of the capacitor leads converter output voltage to drop below specifications affecting downstream components.
- In some cases, the combined effects of the voltage drop and the ripples may damage the converter and downstream components leading to cascading failures in systems and subsystems

# ALUMINUM E-CAPS

## WEAROUT MODEL AVAILABLE IN LITERATURE



Source: NIPPON Chemi-Con Technical Note
“Judicious Use of Aluminum Electrolytic Capacitors”

**Arrhenius-like model** (effect of temperature)

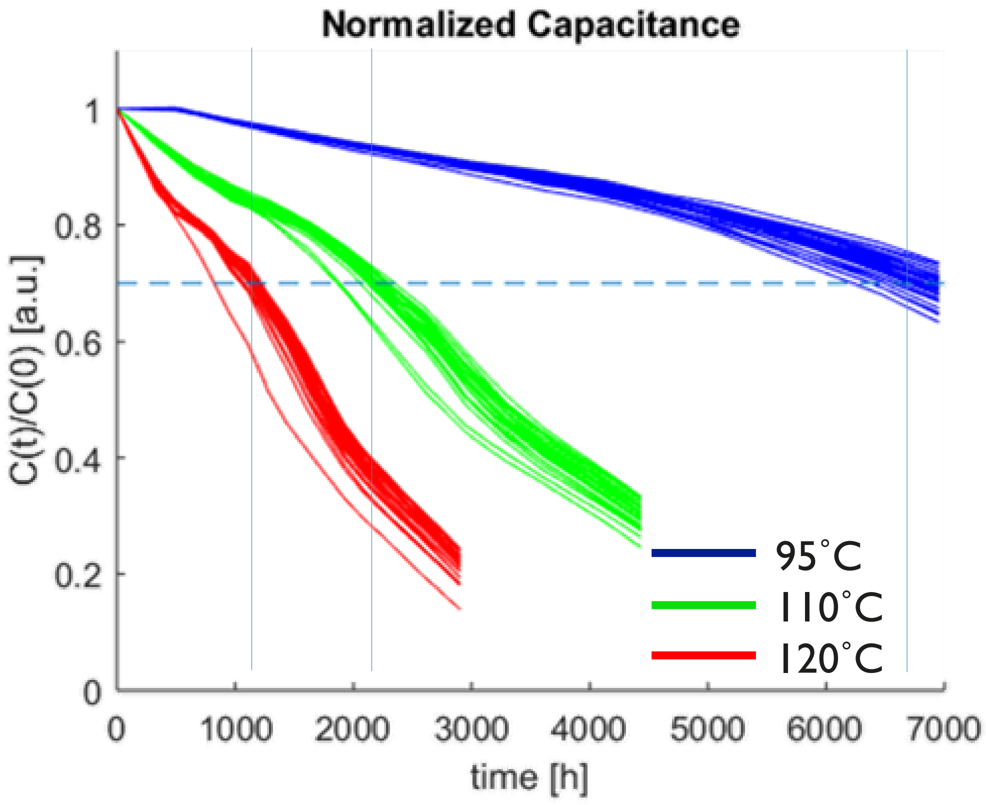
$$t = t_0 \; exp\left[\frac{E_a}{k}\left(\frac{1}{T_{core}} - \frac{1}{T_0}\right)\right]$$

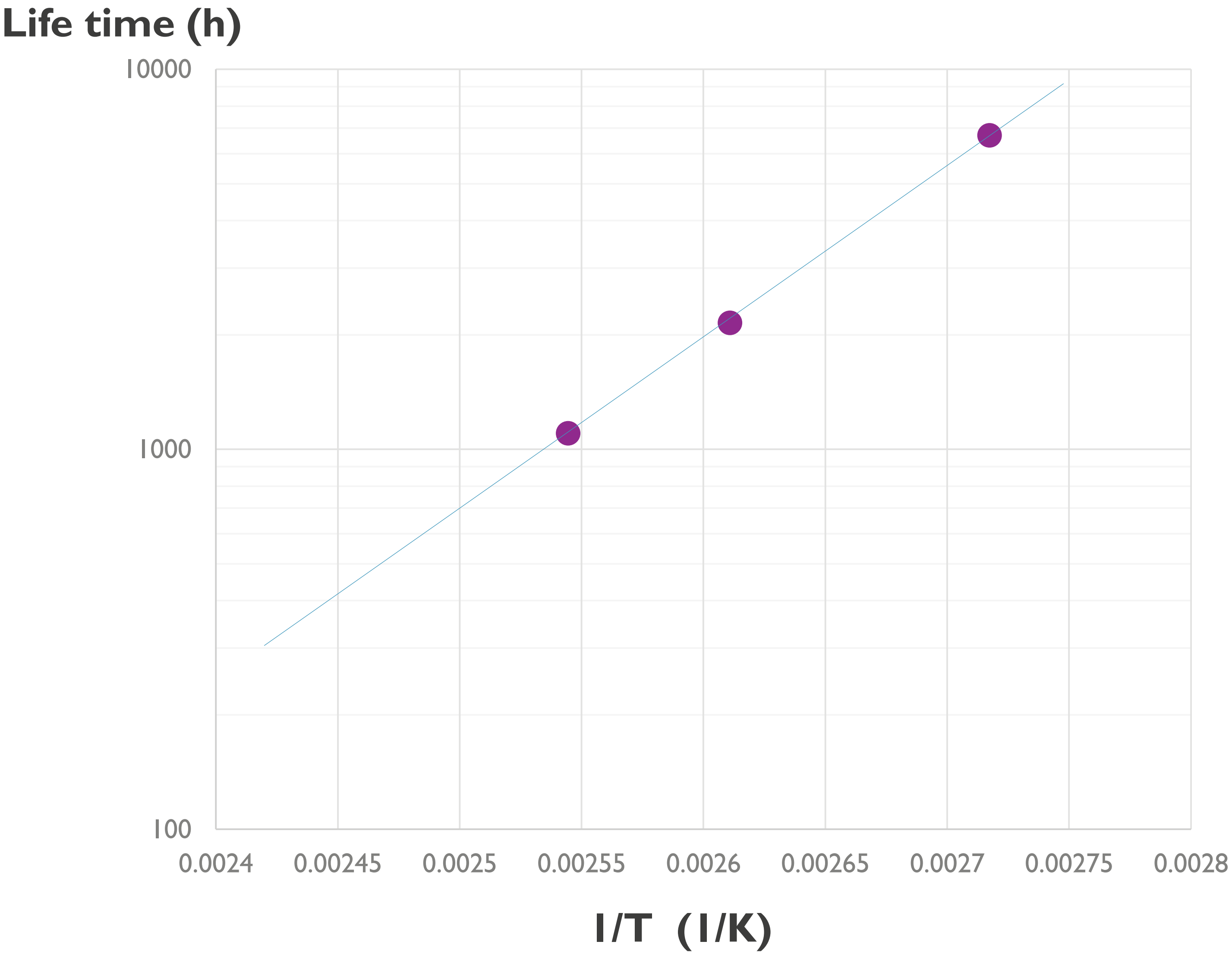
t : estimated lifetime at application conditions
$t_0$ : reference lifetime at $T_0$
$T_{core}$ : application temperature: ambient temperature and ripple effect
$T_0$ : specified maximum temperature
$E_a$ : activation energy [0.79÷0.94 eV]
k : Boltzmann’s constant [$8.62 \times 10^{-5}$ eV/K]

$$T_{core} = T_{amb} + \Delta T_{ripple}$$

$$\Delta T_{ripple} = \frac{{i_{AC}}^2 \tan\delta}{\beta\, A\, \omega C}$$

# OWN MEASUREMENTS CONFIRM THE ARHENIUS MODEL

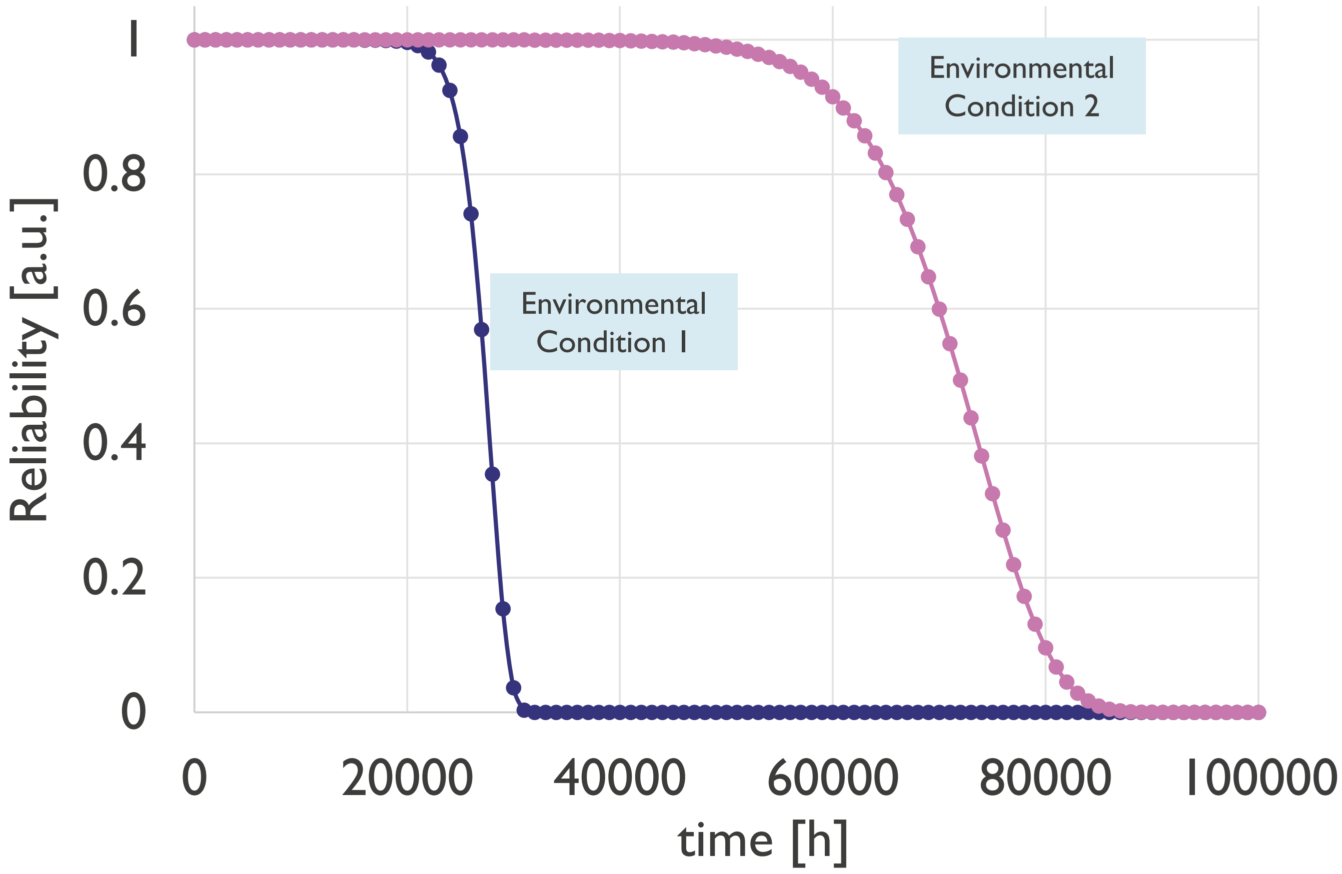




# CONSIDERATION REGARDING POF MODEL

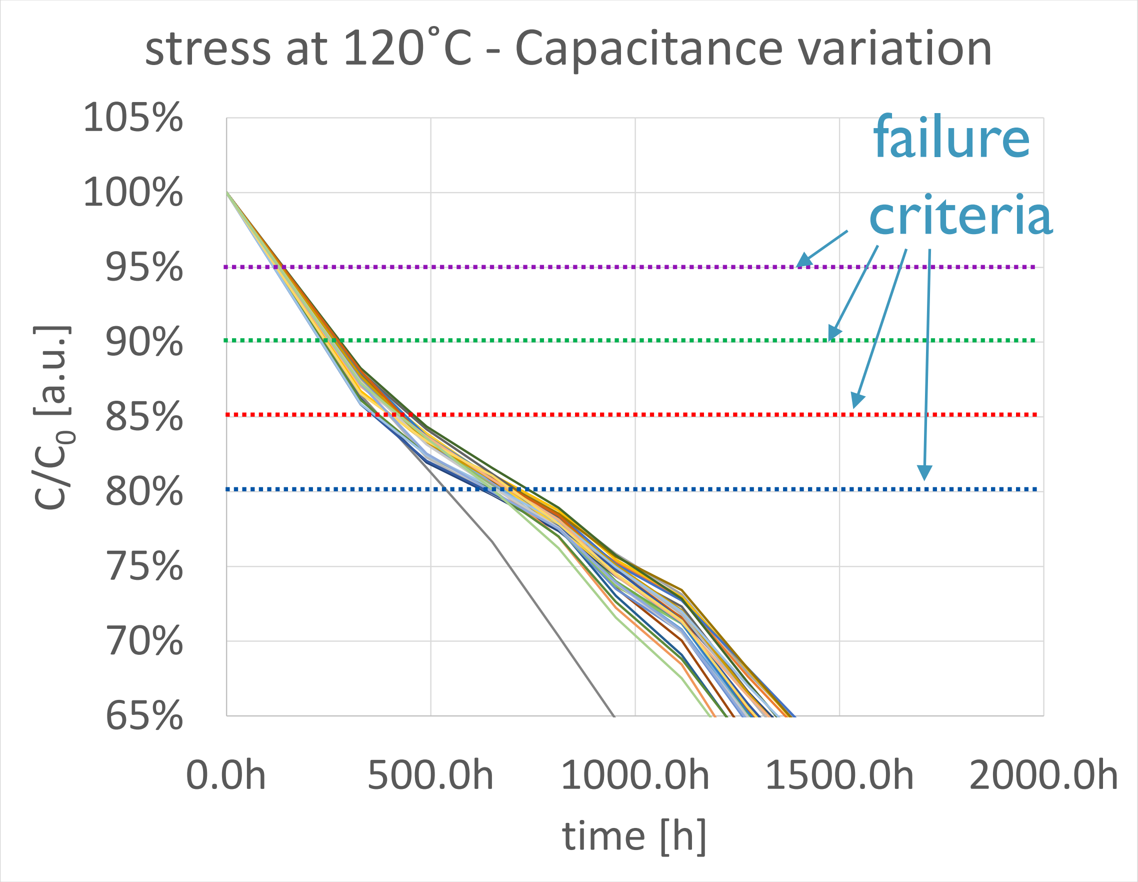
1. Dealing with reliability, not only life time

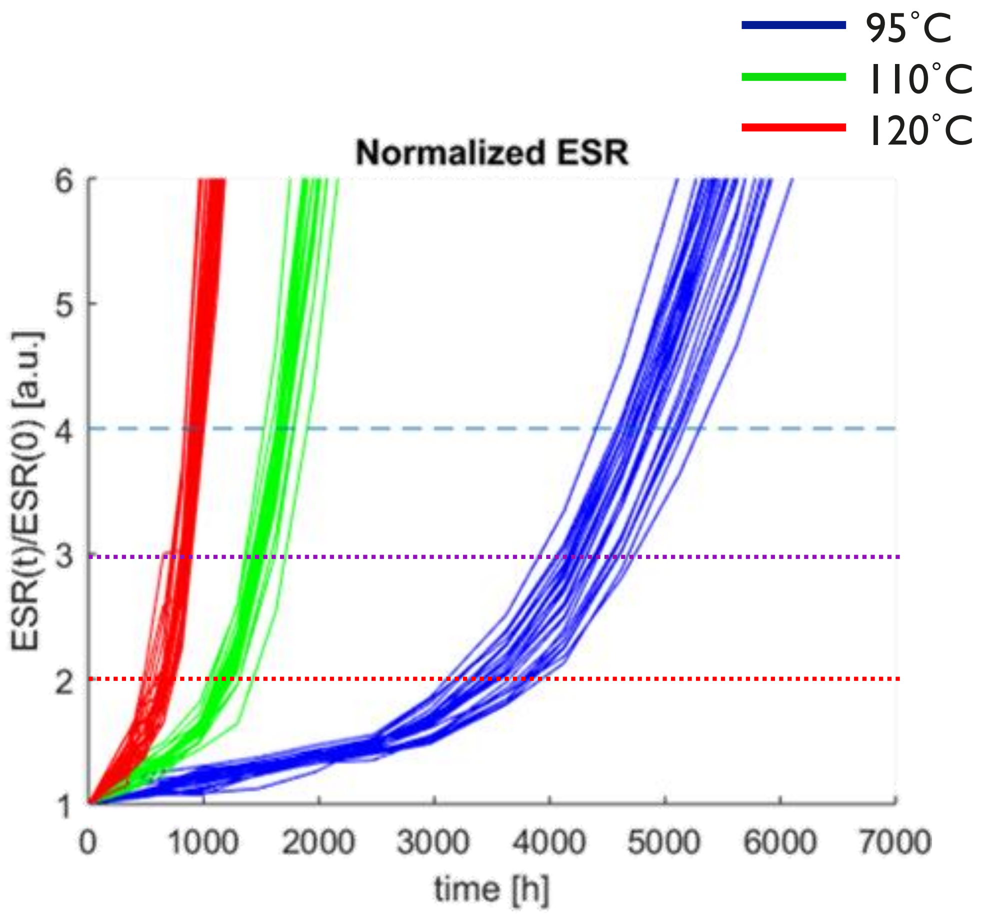
**Reliability 0≤*R(t)*≤*1*** of an item is the probability of having no failure up to time *t*.



# CONSIDERATION REGARDING POF MODEL

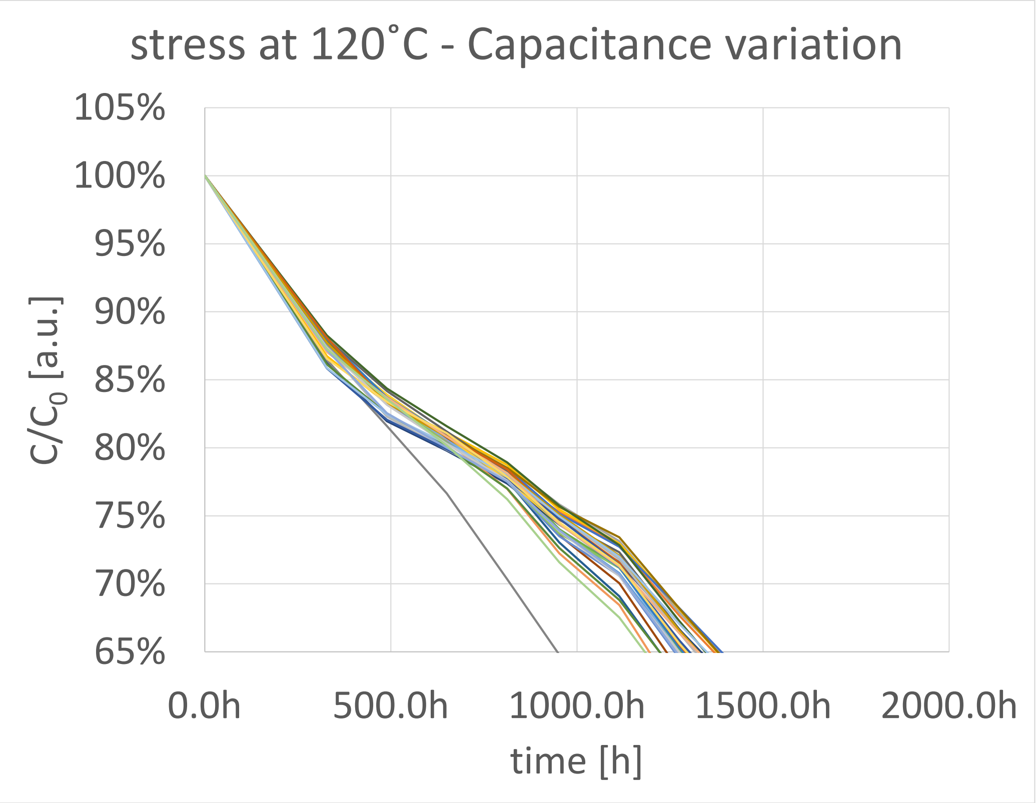
1. Dealing with reliability, not only life time
2. Failure criteria and definition dependent



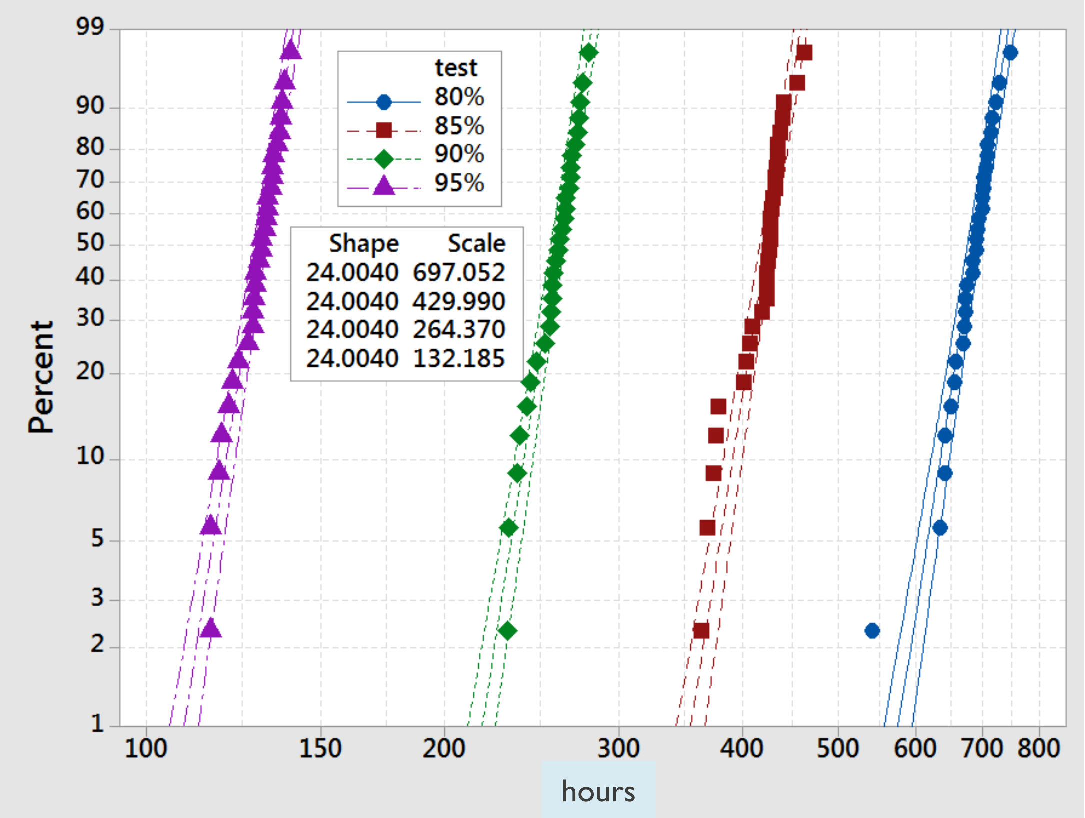


# CONSIDERATION REGARDING POF MODEL

1. Dealing with reliability, not only life time
2. Failure criteria and definition dependent
3. Need to deal with statistics


stress at 120˚C - Capacitance variation

2 parameter Weibull plot

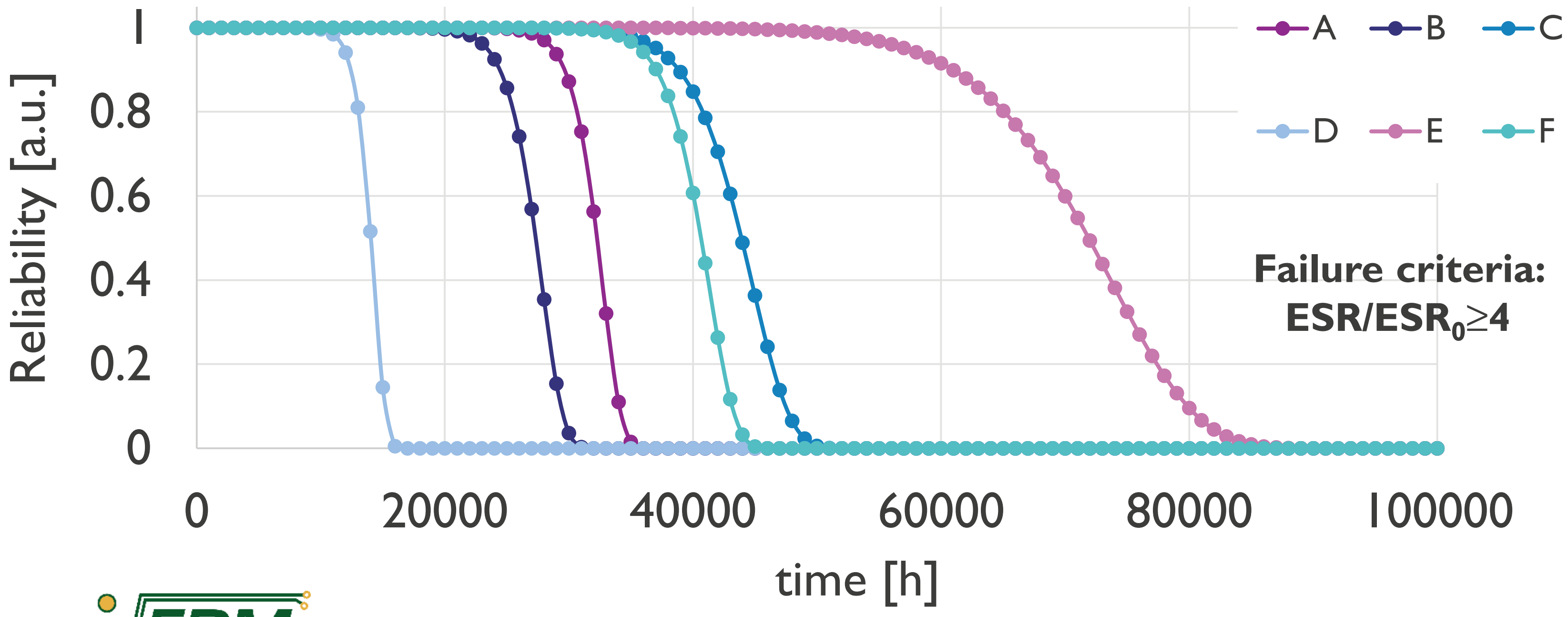


| Shape | Scale |
|---|---|
| 24.0040 | 697.052 |
| 24.0040 | 429.990 |
| 24.0040 | 264.370 |
| 24.0040 | 132.185 |

# CONSIDERATION REGARDING POF MODEL

1. Dealing with reliability, not only life time
2. Failure criteria and definition dependent
3. Need to deal with statistics
4. Parameters are varying for different components and suppliers: need for measurements

EXAMPLE: RELIABILITY AT $T_{CORE}$=70°C (BASED ON EXTRAPOLATION OF MEASURED CURVES)



**Failure criteria:**
**$ESR/ESR_0 \geq 4$**

6 components providing **equal** life time according to their datasheet

# TYPICAL FLOW

Operational temperature & voltage

→

PoF model:
$C(t)/C_0$
$ESR(t)/ESR_0$

→

Failure criteria:
$C(t)/C_0 < Crit1$
$ESR(t)/ESR_0 < Crit2$

→

Reliability
$= f(t)$

# OUTLINE

1. The PoF vs. the statistical approach for reliability prediction

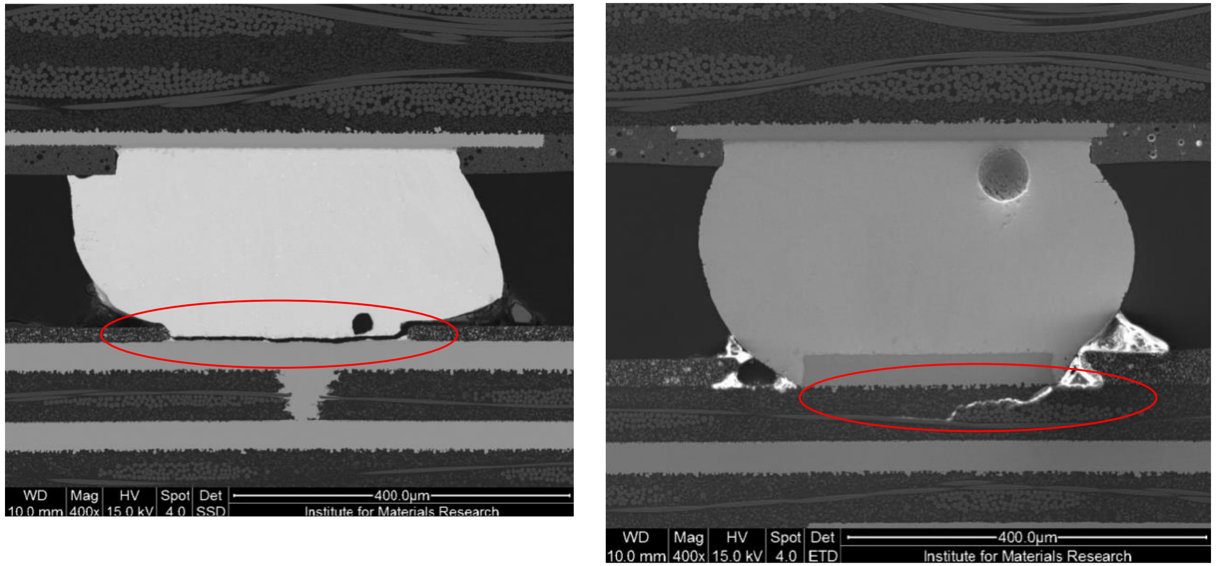
2. Practical Models based on analytical equations:
   - Via fatigue model: an alternative for IPC Engelmaier model
   - Solder fatigue of components on PCB's
   - Al capacitor failures

3. Alternative PoF based testing approaches
   - Shock resistance of solder interconnects
   - 4pt bending instead of thermal cycling

# SHOCK RESISTANCE OF SOLDER INTERCONNECTS

# MOTIVATION

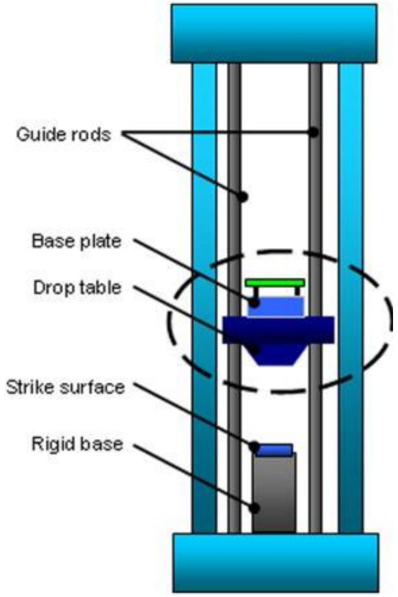
- Increasing amount of brittle fracture failures due to
  - More rigid solder compositions (SnAgCu alloys with additional elements to increase the creep resistance)
  - More quality issues, in particular with NiAu finishes
  - Increased use of BGA's, also for handheld applications

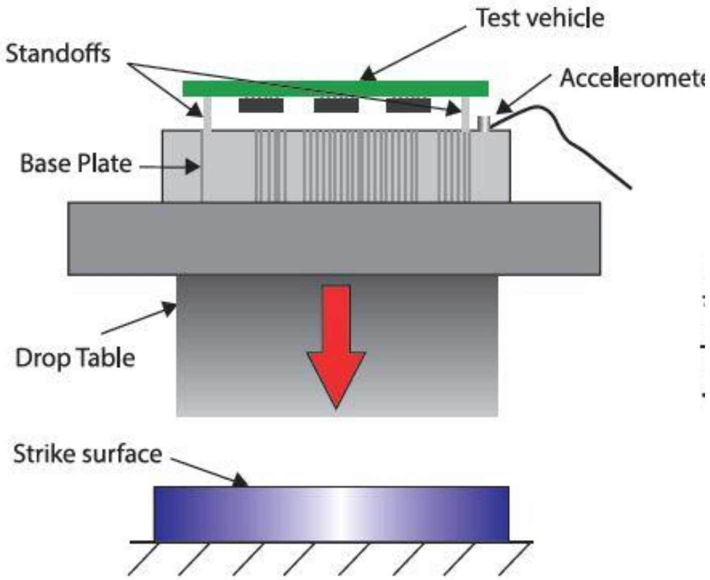


IMC fracture

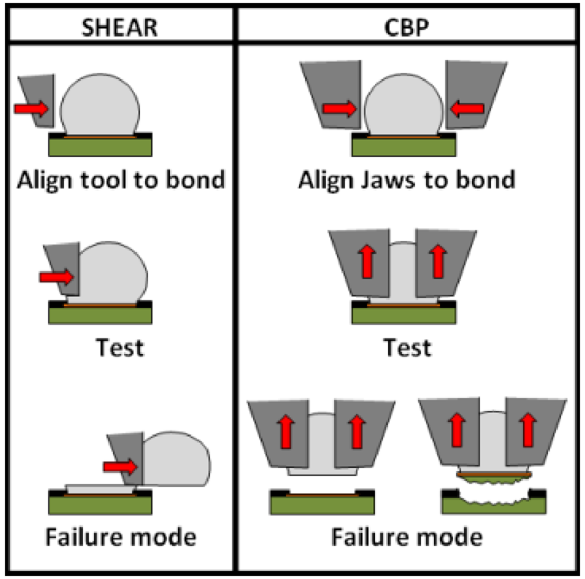
# COMMON METHODS FOR SHOCK TESTING

IPC9703/**JEDEC**-JESD22-B111





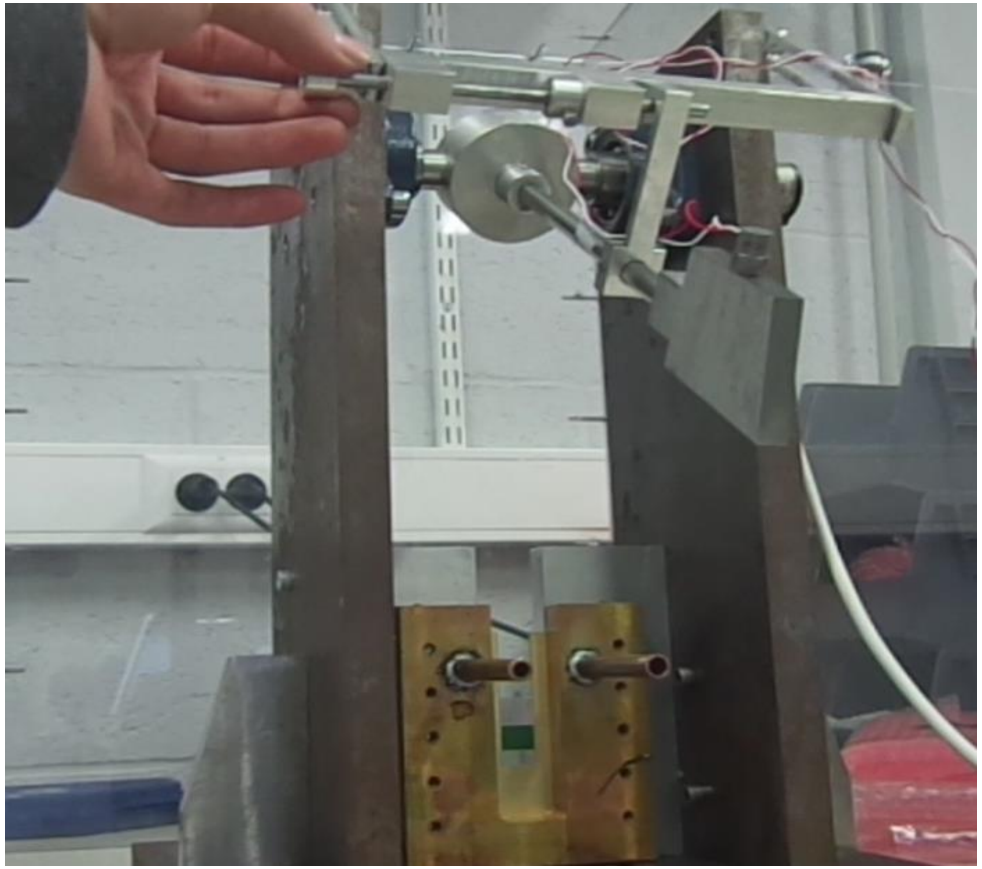
High strain rate ball shear/pull tests

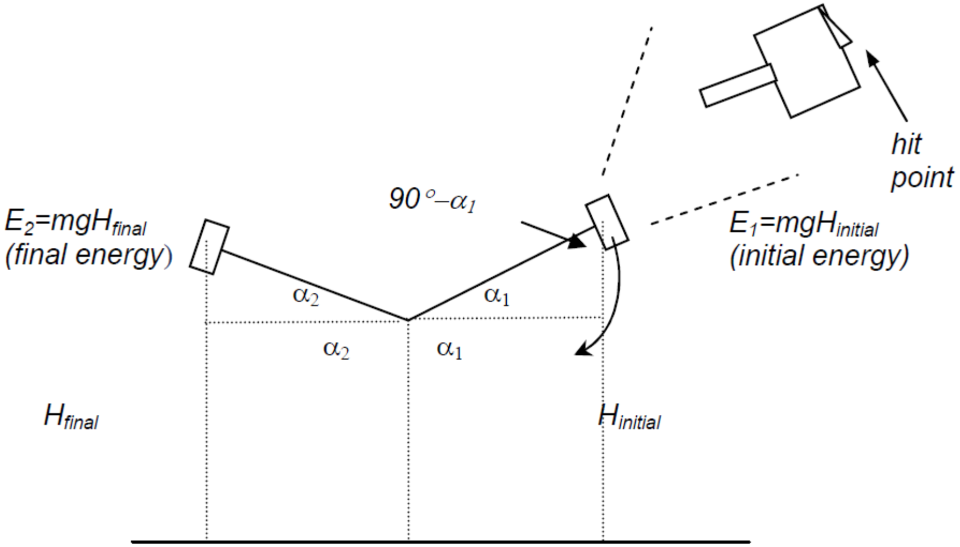


- **Combined shear and pull loading**
- **Mainly qualitative test (no quantitative data about shock resistance for specific solder/finish combination)**

- **Quantitative data**
- **Shear shock is less relevant**
- **Pull shock is difficult to perform at sufficient high strain rates**

# POF BASED APPROACH FOR SHOCK TESTING





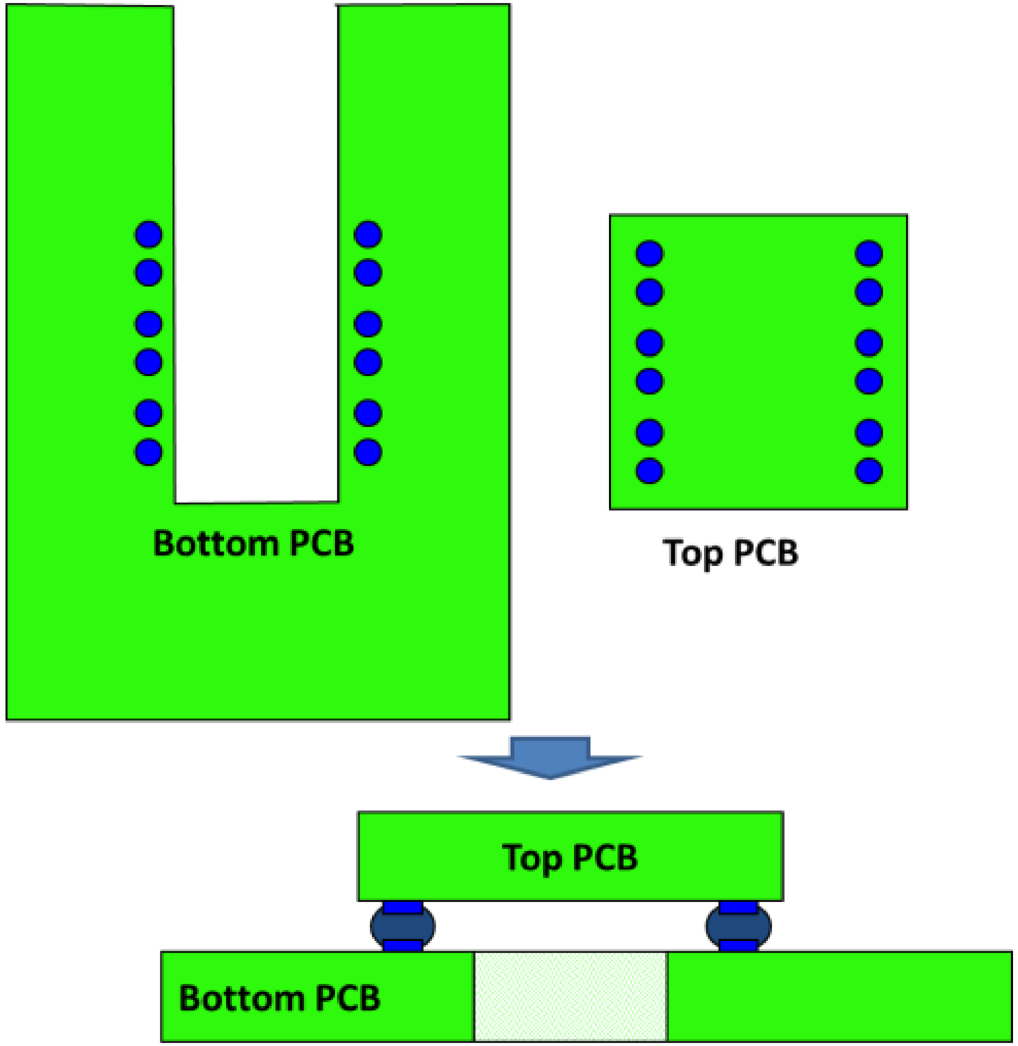
**Measured output:**

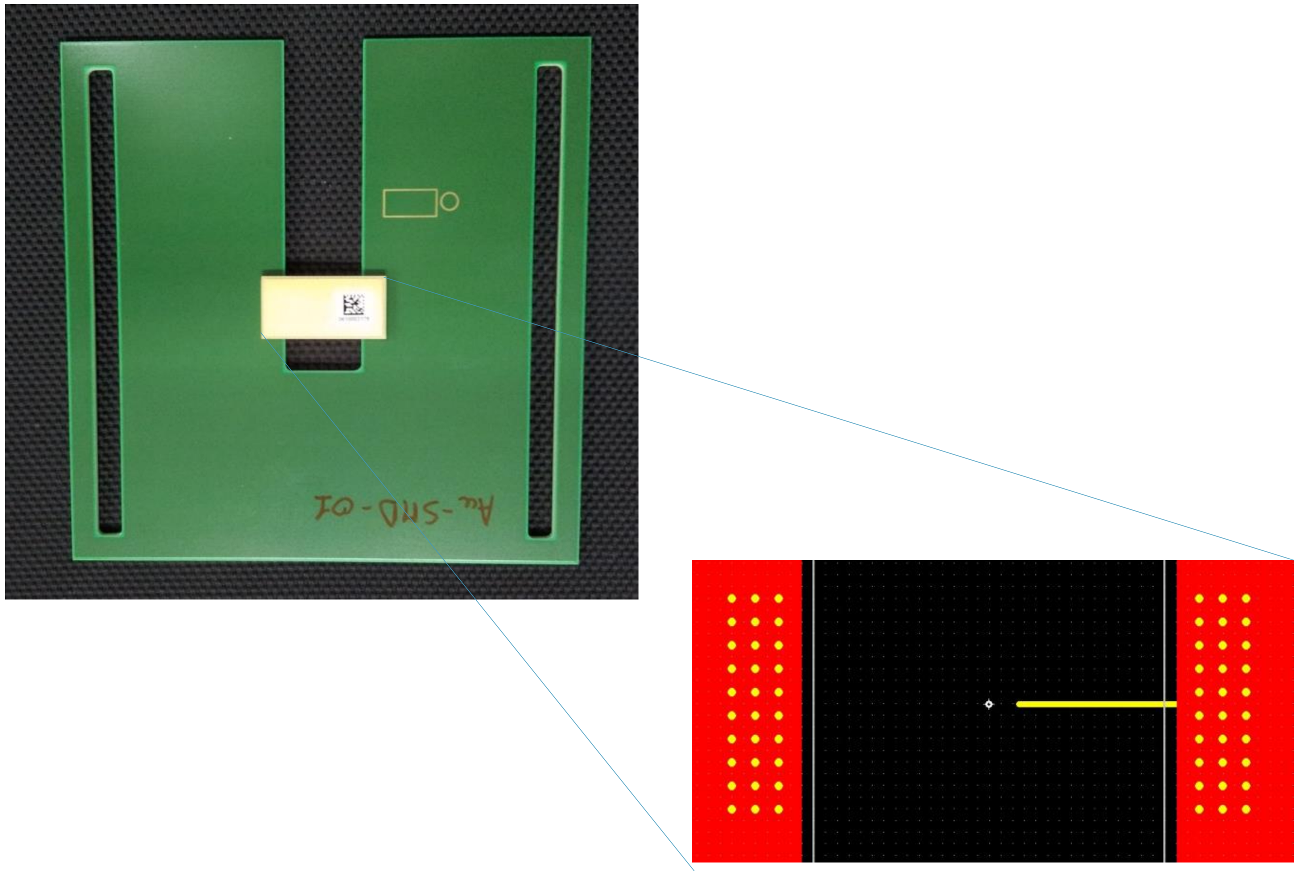
- Energy taken up by the sample
- Maximum force before fracture

**Additional features:**

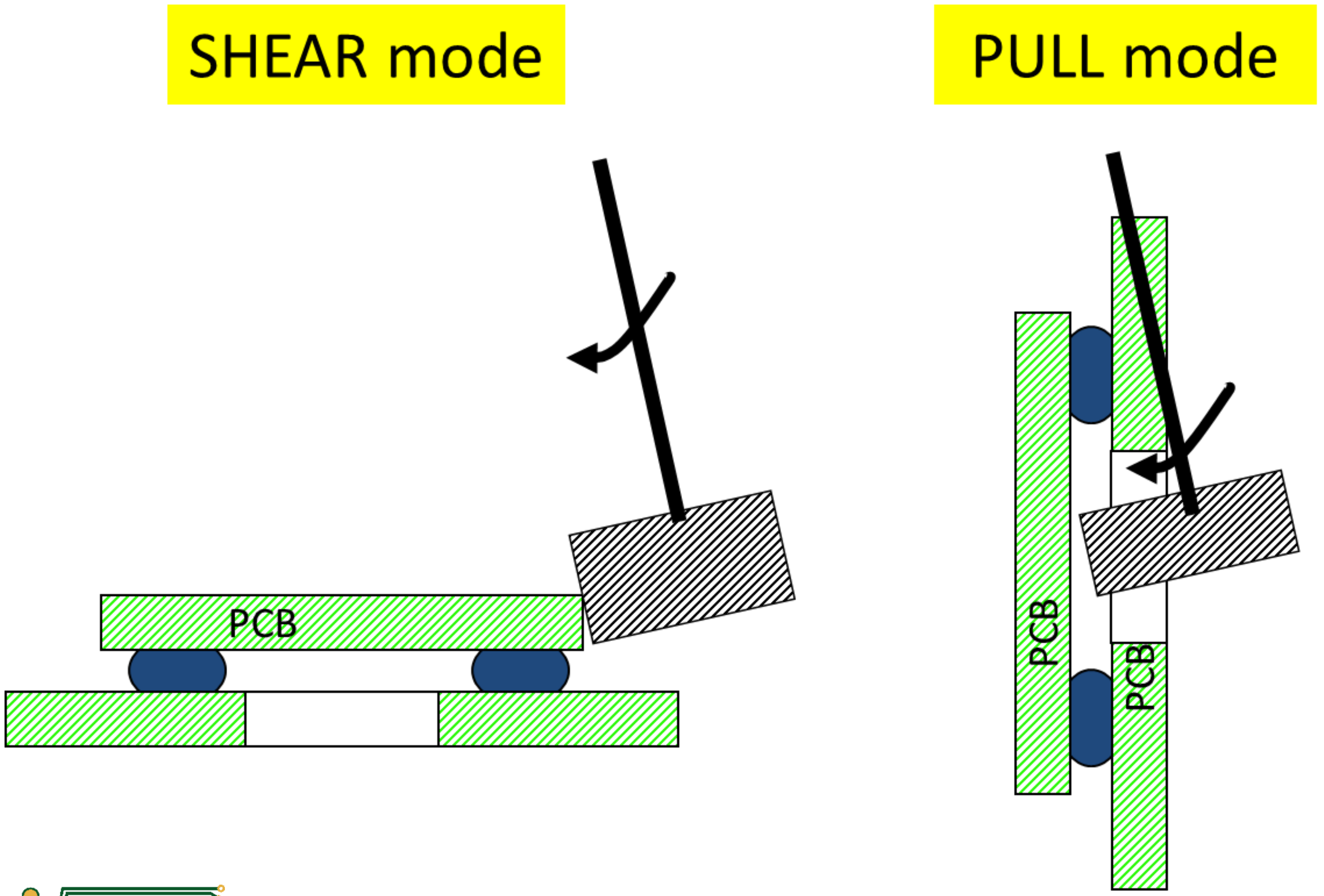
- Cooling is possible (e.g. measurement @-40°C)

# SAMPLE DESCRIPTION

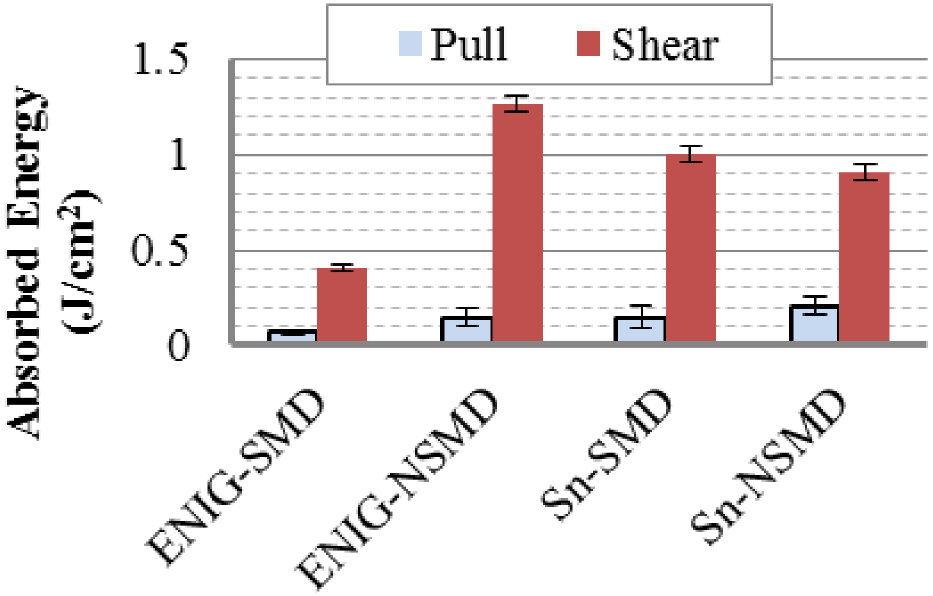


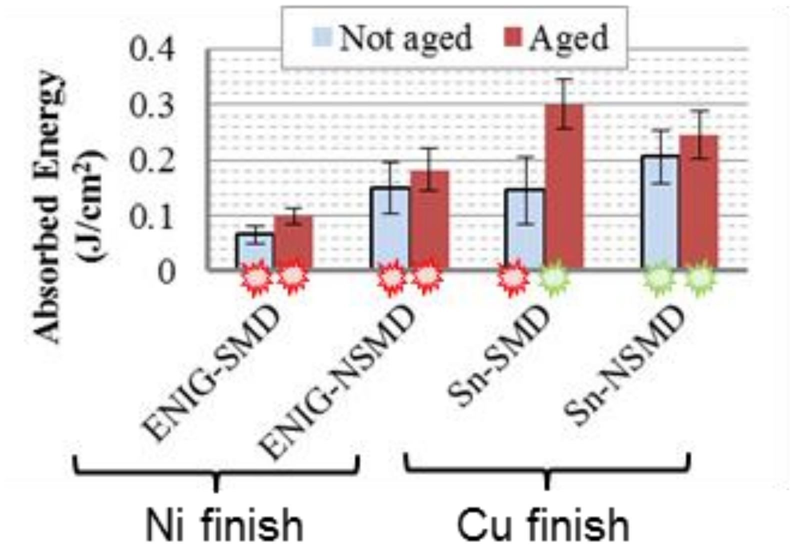


# SPECIAL SAMPLE DESIGN ALLOWS FOR TESTING ALSO IN PULL MODE

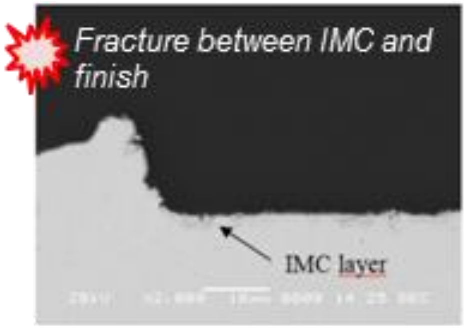


# RESULTS FOR DIFFERENT FINISHES

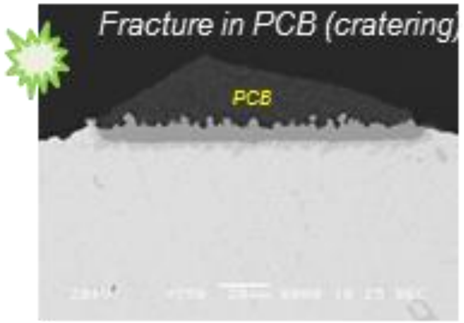




Ageing conditions: 1000 hours @150°C



*Fracture between IMC and finish*

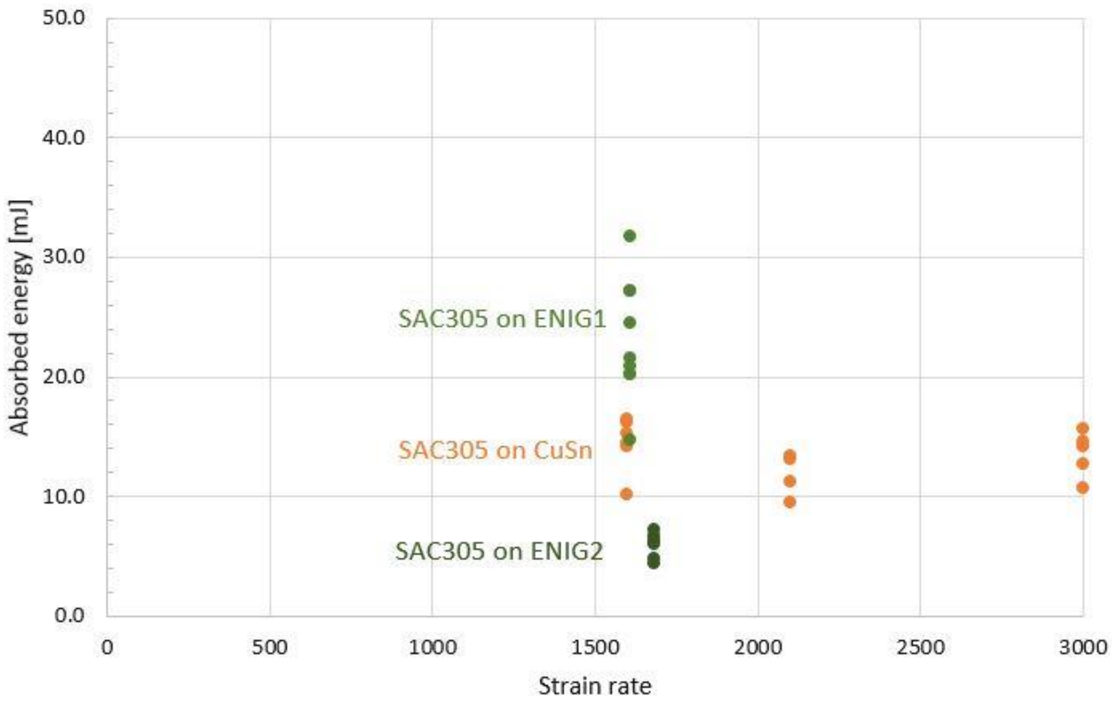


*Fracture in PCB (cratering)*

Solder joints are much more sensitive to **pull** shock

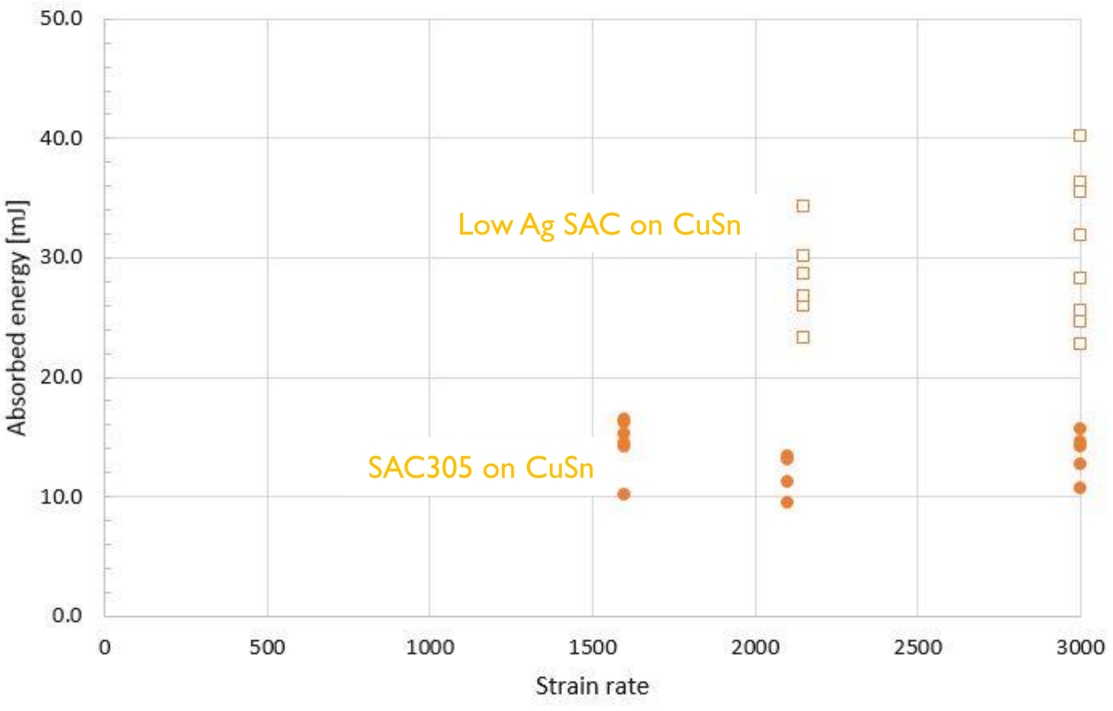
Solder joints on **Ni** have up to **50% lower** resistance to mechanical shock compared to joints on **Cu** based finishes

# RESULTS FOR DIFFERENT FINISHES (2)



- **Conclusions:**
  - Shock resistance of solder joints on ENIG can also be better than on Cu based finish (HASL, Sn, Ag)
  - Difference in ENIG strength experienced between suppliers (factor 5 !!!)

# RESULTS FOR DIFFERENT SOLDER COMPOSITIONS



- **Conclusions:**
  - Reducing the Ag content in solder improves the shock resistance of interconnects

# 4PT BENDING INSTEAD OF THERMAL CYCLING

# THERMAL CYCLING (TC) EXPERIMENTS

## RELEVANCE AND DRAWBACKS

Relevance:

- Thermal cycling testing is a widely spread method for analyzing the board level thermal cycling performance of printed board assemblies
  - Thermal cycling mimics the temperature swings the electronic systems sees during its operational life
  - Thermal cycling testing is part of basically all qualification standards

Drawbacks:

- TC testing is a time consuming experiment
- Acceleration of the test through:
  - Higher temperature swing ($\Delta T$) by increasing the $T_{max}$ and/or decreasing the $T_{min}$
    - Risk for inducing new failure modes which may be not relevant for the operational conditions the system has to work
  - Reducing the cycle time
    - Solders need time to fully relax. This is even more relevant for lead-free solders
    - The thermal mass of the equipment needs time to heat up or cool down

# THERMAL CYCLING: WHAT IS REQUIRED?
# SOME FIGURES FOR REFERENCE (IPC-9701)

**Computer and peripherals:** ΔT=20K, 4cpd, 5y, 0.1%

- N63%(0-100°C) → 1250 cycles/5y

**Telecom:** ΔT=35K, 1cpd, 7-20y, 0.01%

- N63%(0-100°C) →
  >2000 cycles/7y...6000 cycles/20y

**Industrial/automotive:** ΔT=20K(50%)/40K(27%)/60K(16%)/80K(6%), 365cpy, 10-15y, 0.1%

- N63%(0-100°C) → >3000 cycles/10y...4500 cycles/15y

**Commercial aircraft:** ΔT=20K, 1cpd, 20y, 0.001%

- N63%(0-100°C) → 3500 cycles/20y

**Military:** ΔT=40K(27%)/60K(73%), 365cpy, 10-20y, 0.1%

- N63%(0-100°C) → 5500 cycles/10y...11000 cycles/20y

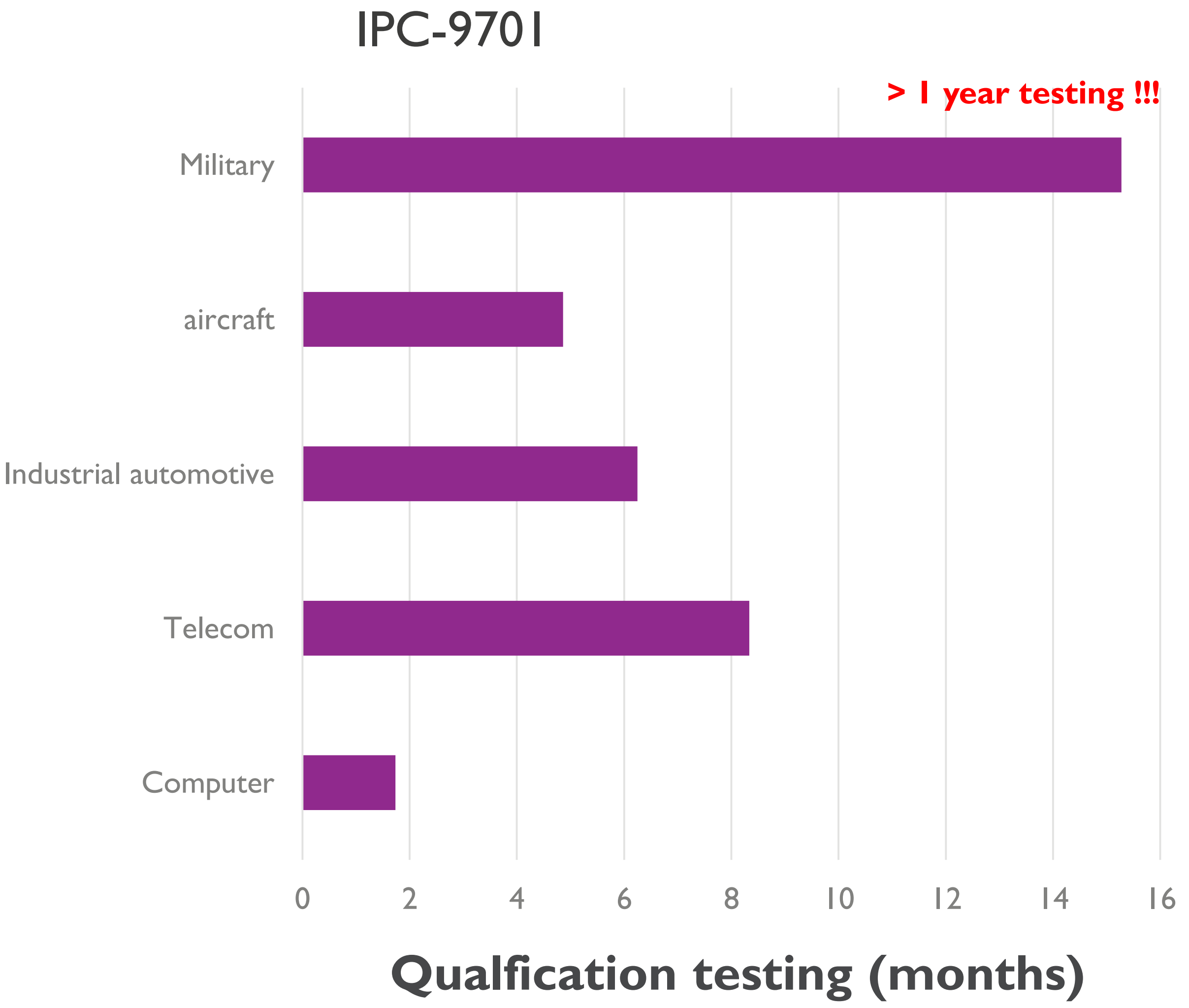
Notes:
- Acc. Factor: SnPb Norris-Landzberg eq.
- Weibull slope=6
- No power cycling
- Tmax= max. operation

# LIMITATIONS OF THERMAL CYCLING TESTING FOR BOARD LEVEL RELIABILITY TESTING

- Time consuming: 1 hour per cycle (recommended for leadfree solders)

↓

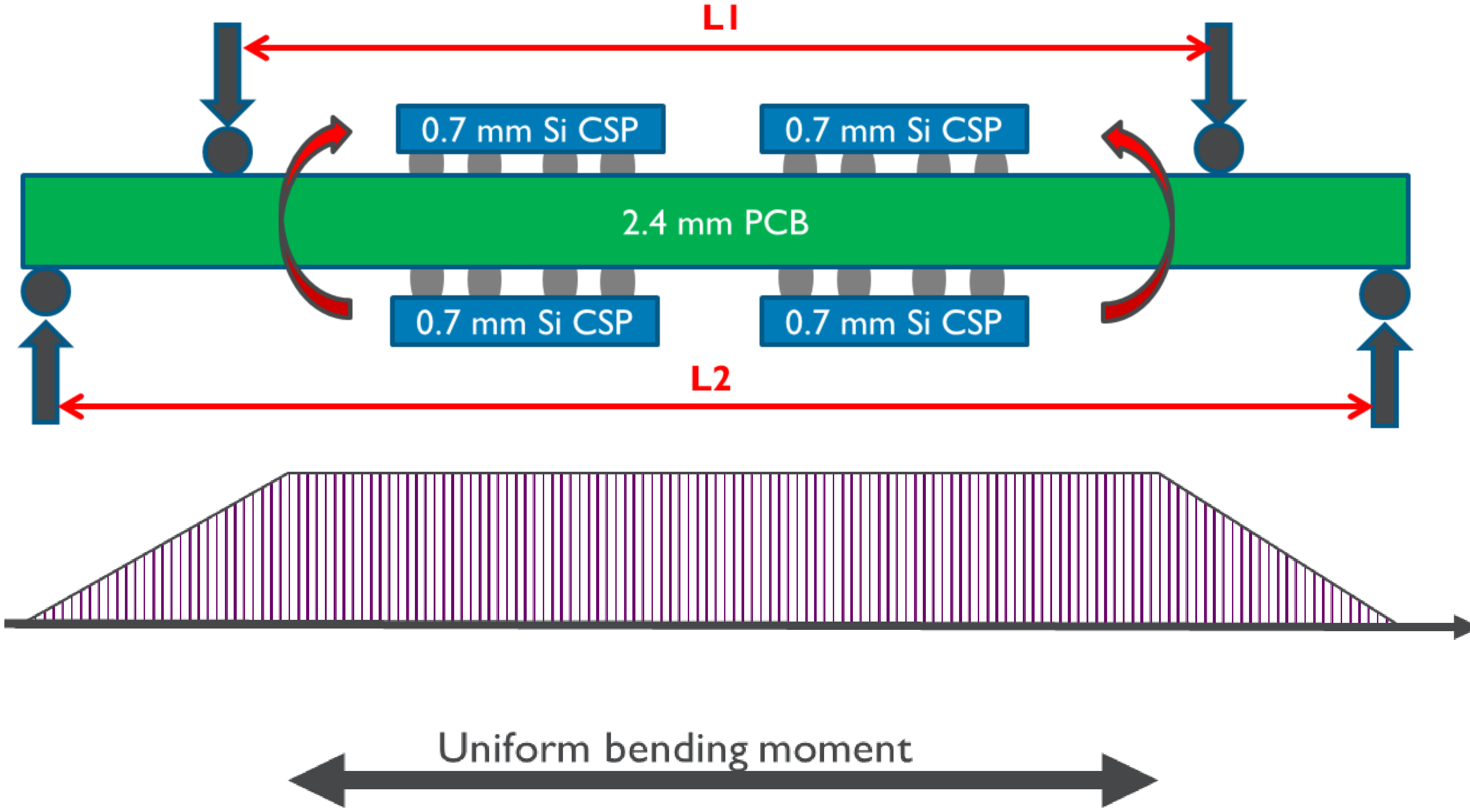
- Alternative test: **4 pt bending fatigue testing at constant temperature**



# ALTERNATIVE FOR TC TESTING: FOUR POINT BENDING

## CONCEPT

- Applying a 4pt bending causes an in-plane deformation at the top and bottom fibre of the PCB
- This results into a relative displacement between component and PCB, similar to the CTE mismatch
- In between the roller bars, the bending moment is constant, so all components are equally stressed



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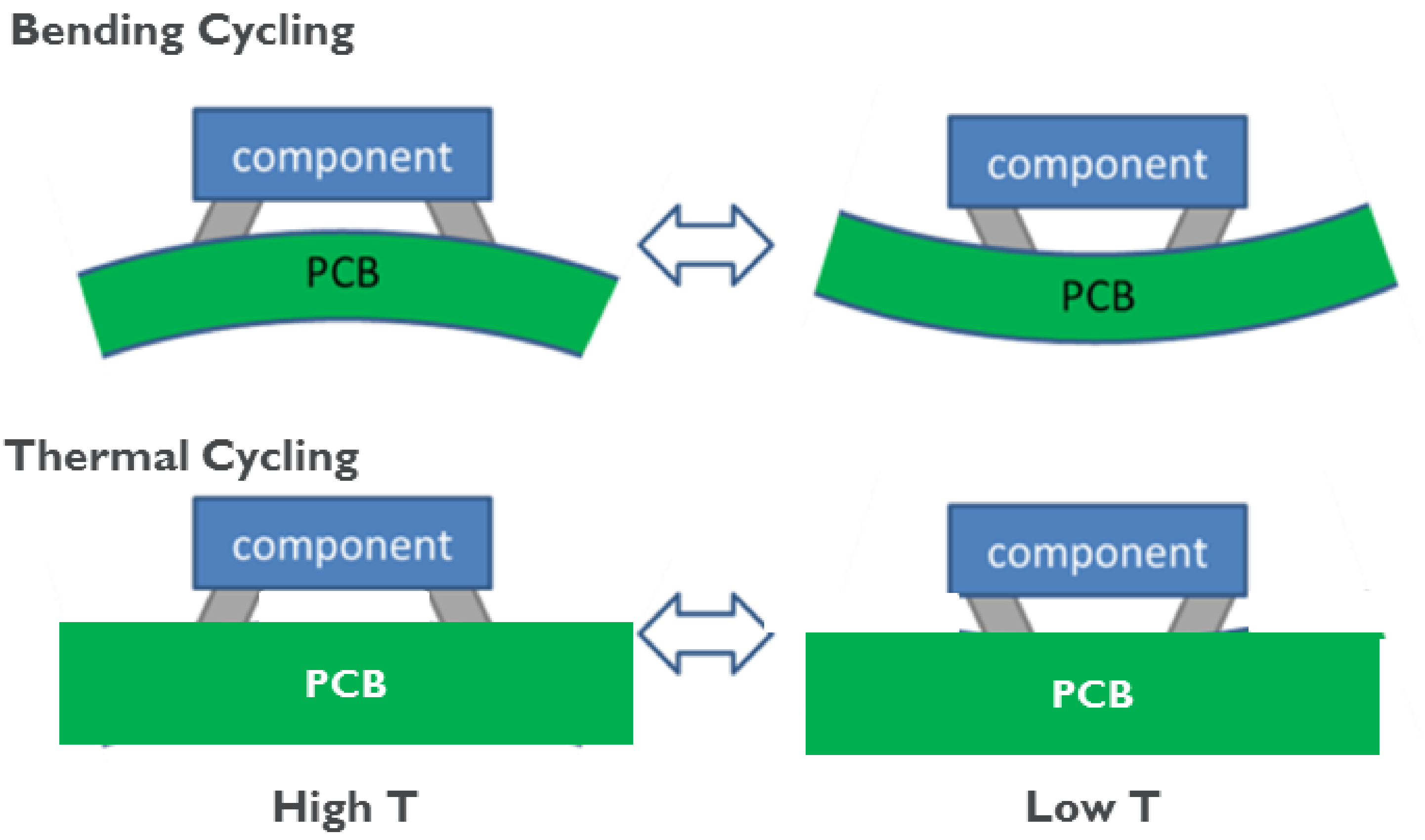
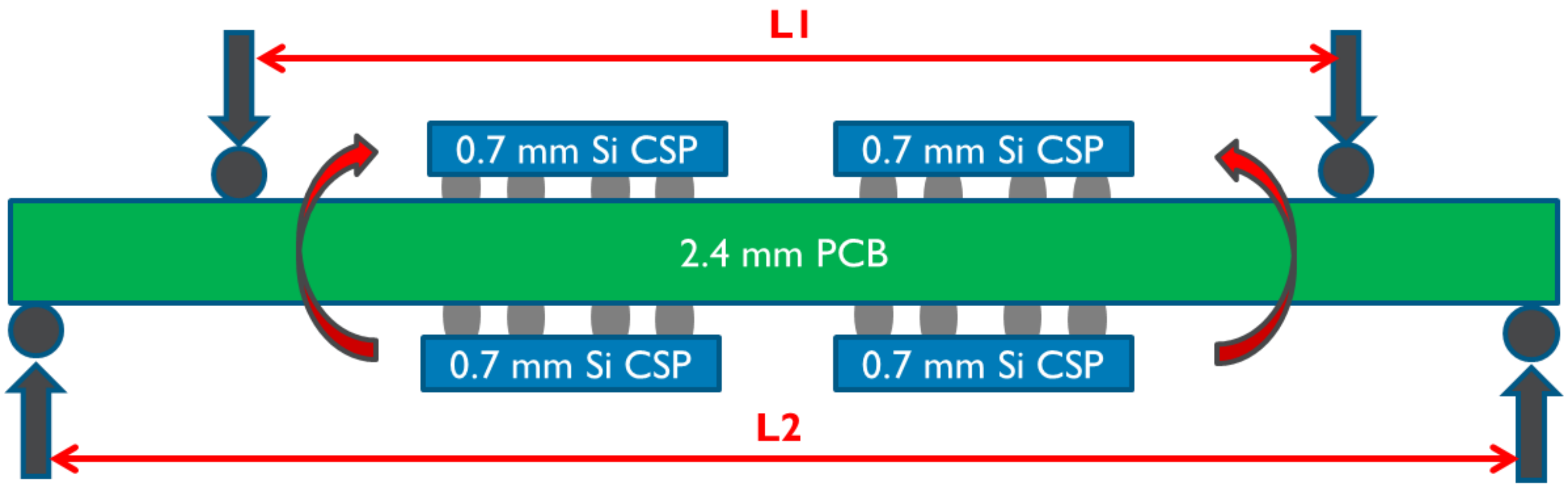


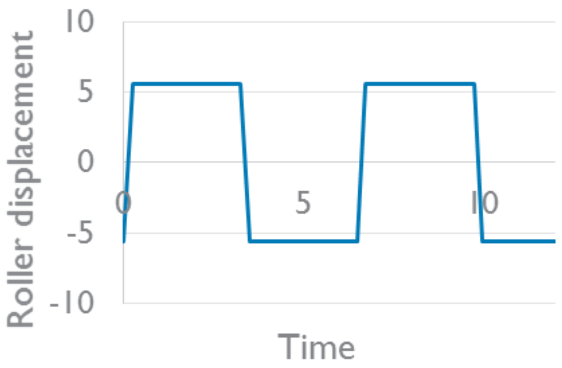
# ALTERNATIVE FOR TC TESTING: FOUR POINT BENDING

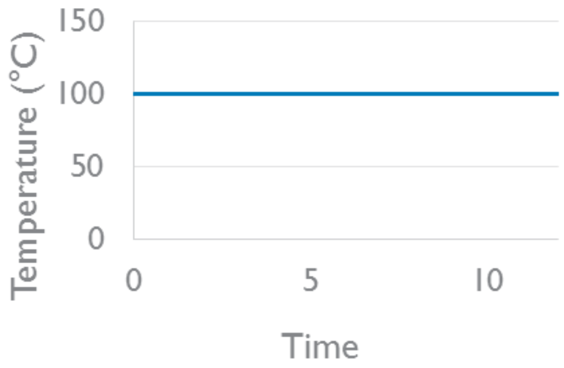
## CONCEPT (2)

Test conditions:

- Temperature is kept constant
- Cycling performed through the roller displacement. Both ramp-up and dwell time can be controlled.

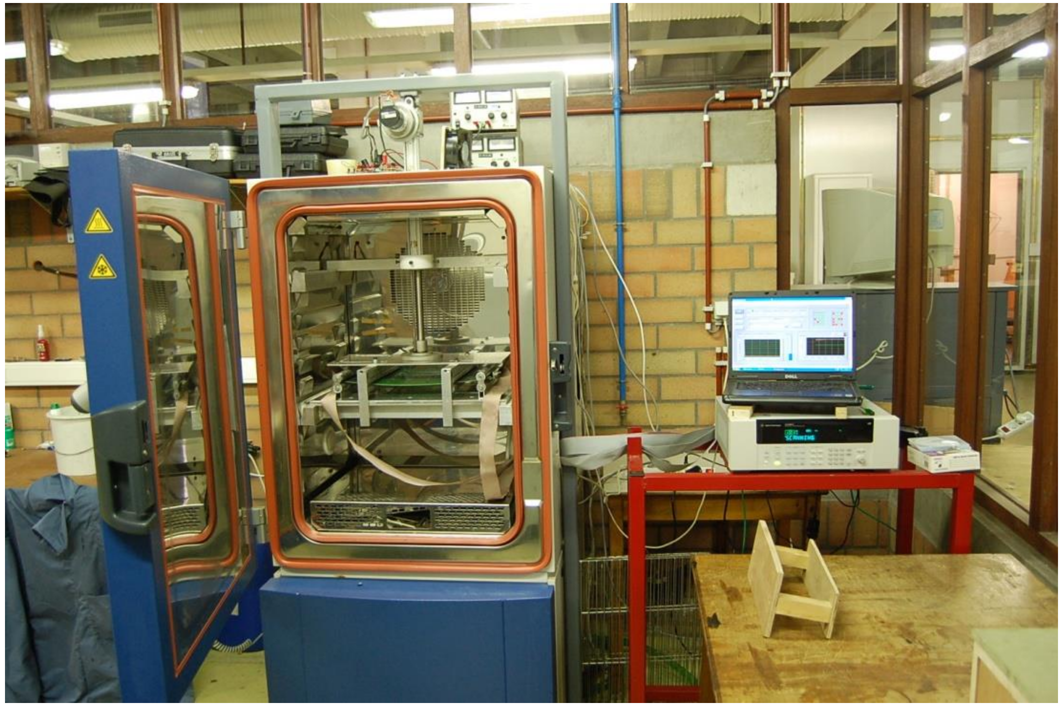






# FOUR POINT BENDING SETUP

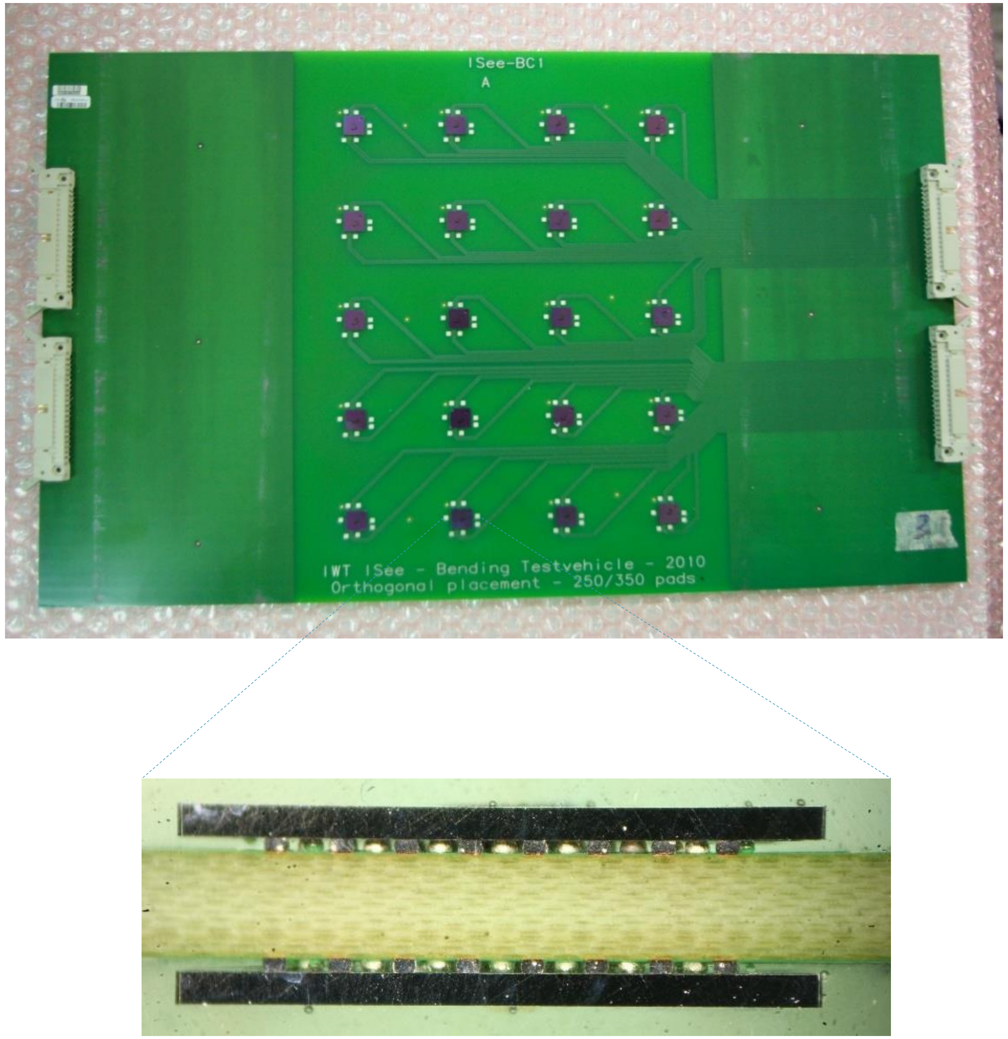
## 4PT BENDING SYSTEM INSIDE THERMAL CHAMBER



# FOUR POINT BENDING SETUP

## TEST VEHICLE

- Test board: 450 mm by 280 mm; 2.5 mm thick
- The daisy chain components are located in the spacing between the load anvils, which is about 210 mm wide
- On each side of the board, 20 daisy chain components have been placed in an array of 4 columns and 5 rows
- Symmetric build-up to guarantee that the neutral fiber remains in the middle of the PCB.



# COMPARISON 4PT BENDING VS. THERMAL CYCLING

## CONDITIONS FOR BOTH TESTS

The same component assembly has been tested under isothermal temperature cycling and 4-point bending cycling.

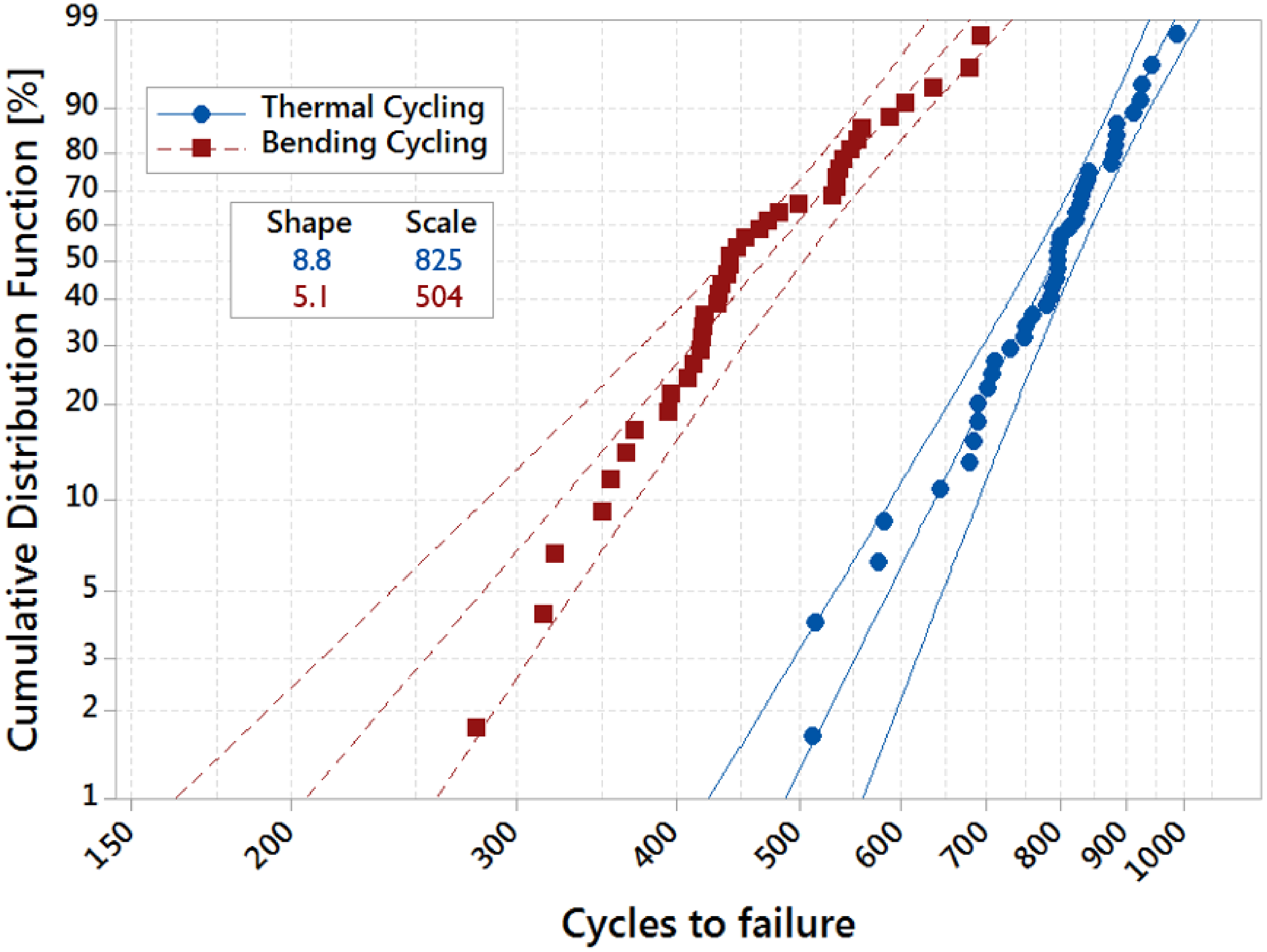
| Test | Conditions | Relative Displacement (DI$_{PCB\text{-}Comp}$) |
|---|---|---|
| **Thermal cycling** | 0 to 100°C cycling<br>20 min dwell time | $\Delta l_{shear} = 6.6\ \mu m$<br>$\Delta l_{normal} \sim 0\ \mu m$ |
| **Bending cycling** | T = 100°C<br>d = 5.6 mm (roller displacement)<br>20 min dwell time | $\Delta l_{shear} = 3.5\ \mu m$<br>$\Delta l_{normal} = 1.8\ \mu m$ |

In this 4 point bending test, a strain is applied equal which loads the solder joint with the same shear displacement as in a thermal cycling with a ΔT of 50°C.

# COMPARISON 4PT BENDING VS. THERMAL CYCLING

## WEIBULL DATA

- 4pt bending cycling results in much earlier failures, although load on the joint is lower
- Slopes (β) of the weibull are similar



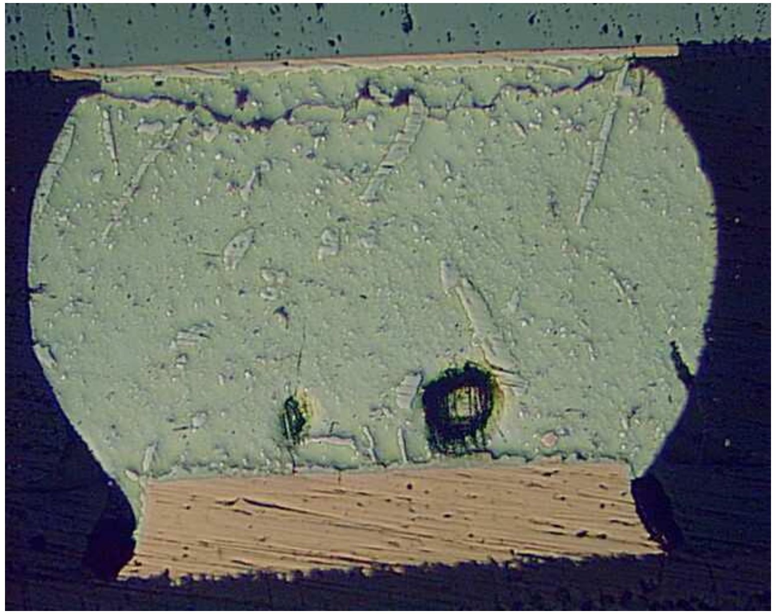
| Shape | Scale |
|---|---|
| 8.8 | 825 |
| 5.1 | 504 |

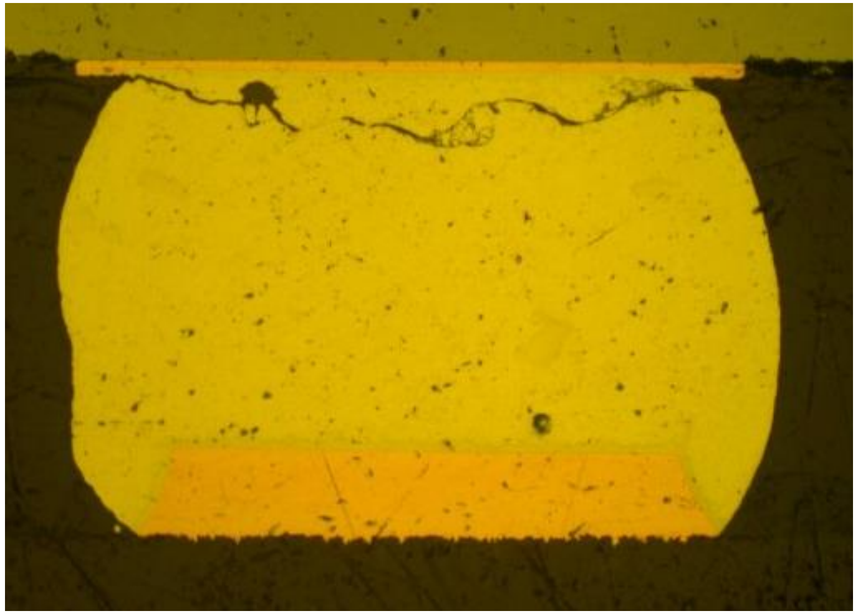
# COMPARISON 4PT BENDING VS. THERMAL CYCLING

## FAILURE ANALYSIS

**Thermal Cycling**

**4pt Bending Cycling**



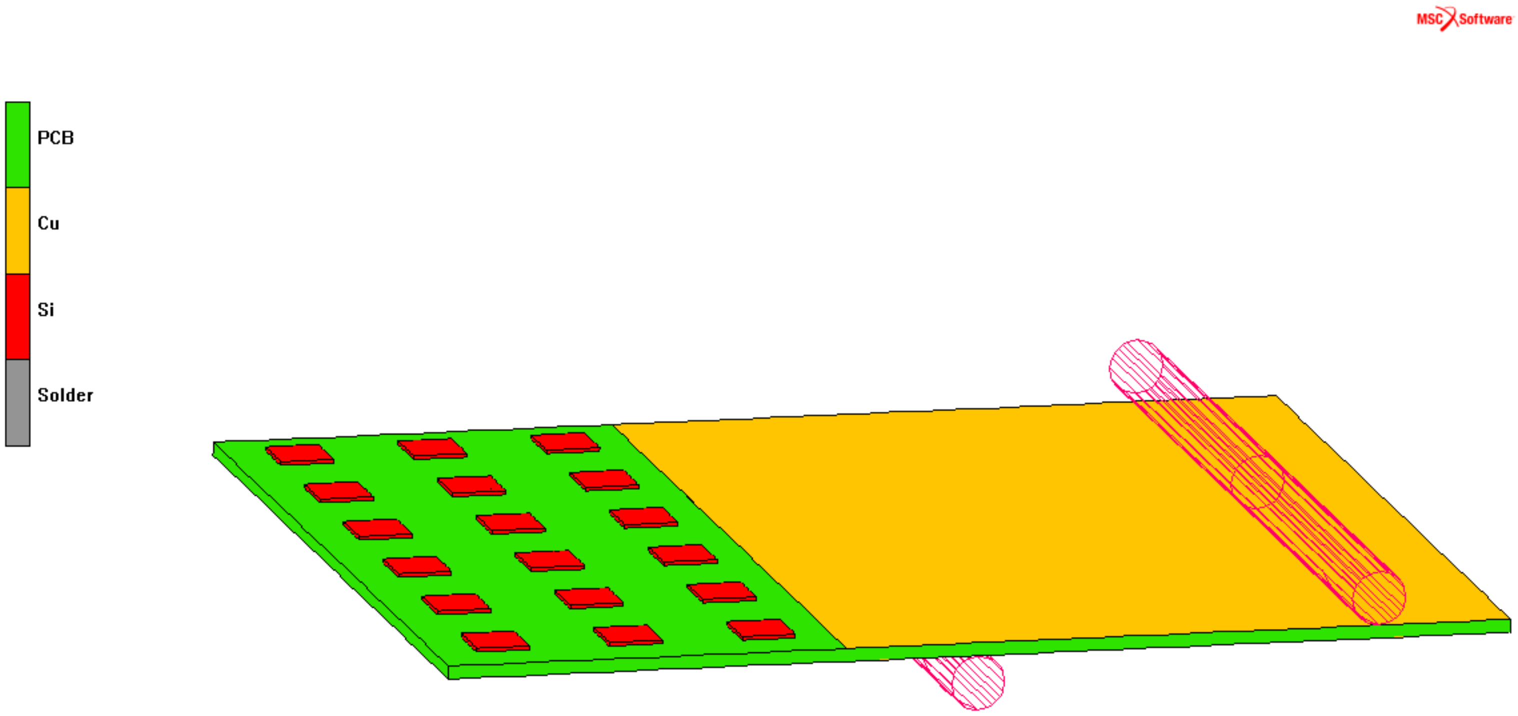


Similar fatigue fracture, located
close to the CSP

# COMPARISON 4PT BENDING VS. THERMAL CYCLING

## EXPLANATION FOR THE HIGHER IMPACT OF 4PT BENDING

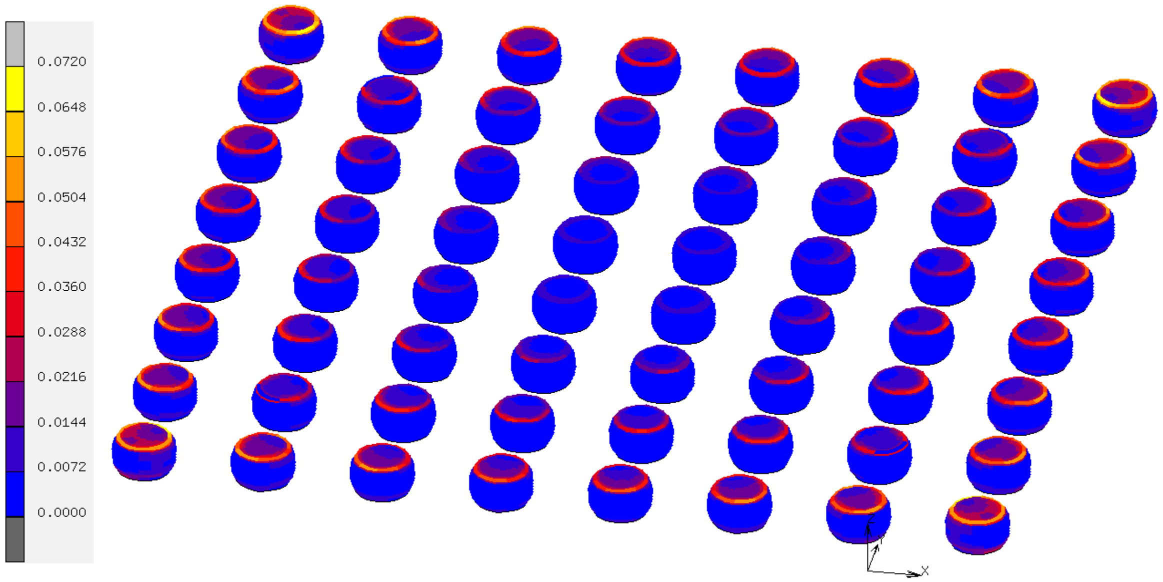
- Finite Element Modelling is used to calculate the strains in the solder joints during TC and 4pt Bending Cycling



# COMPARISON 4PT BENDING VS. THERMAL CYCLING

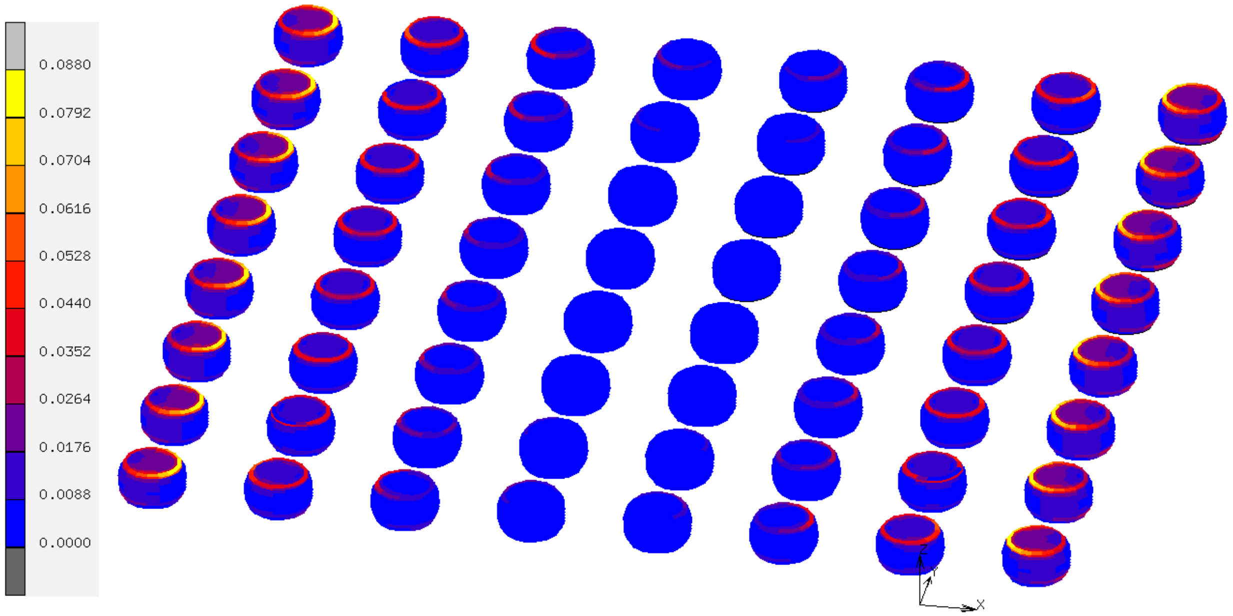
## CREEP STRAIN DISTRIBUTION PER CYCLE

**Thermal Cycling**



Highest strains in the four corners

**4pt Bending Cycling**

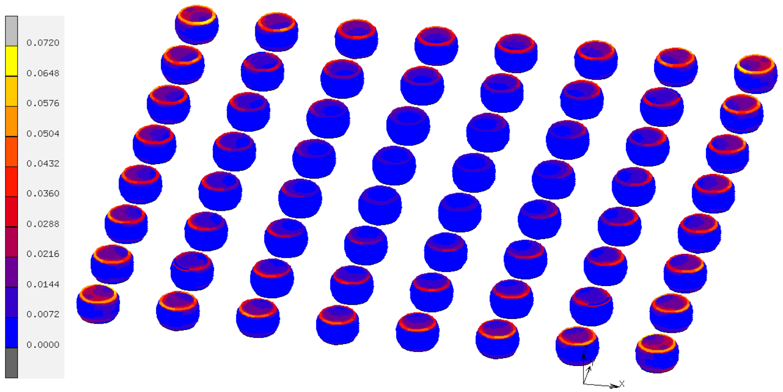


Highest strains in the two outer edges

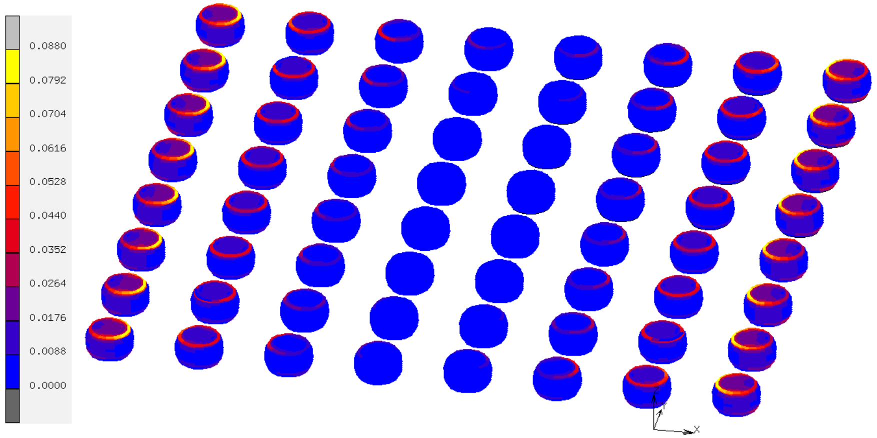
# COMPARISON 4PT BENDING VS. THERMAL CYCLING

## EXPERIMENTS VS. FEM SIMULATIONS

**Thermal Cycling**



**4pt Bending Cycling**



| **Experiments** | **N63% = 804** | **N63% = 500** |
|---|---|---|
| FEM simulation | Max. creep strain = 7.2% | Max. creep strain = 8.8% |

- **Tests at constant 100°C explain the higher creep strains**
- **Simulations are in line with experiments, however the difference is too small to confirm with experiments**

# COMPARISON 4PT BENDING VS. THERMAL CYCLING

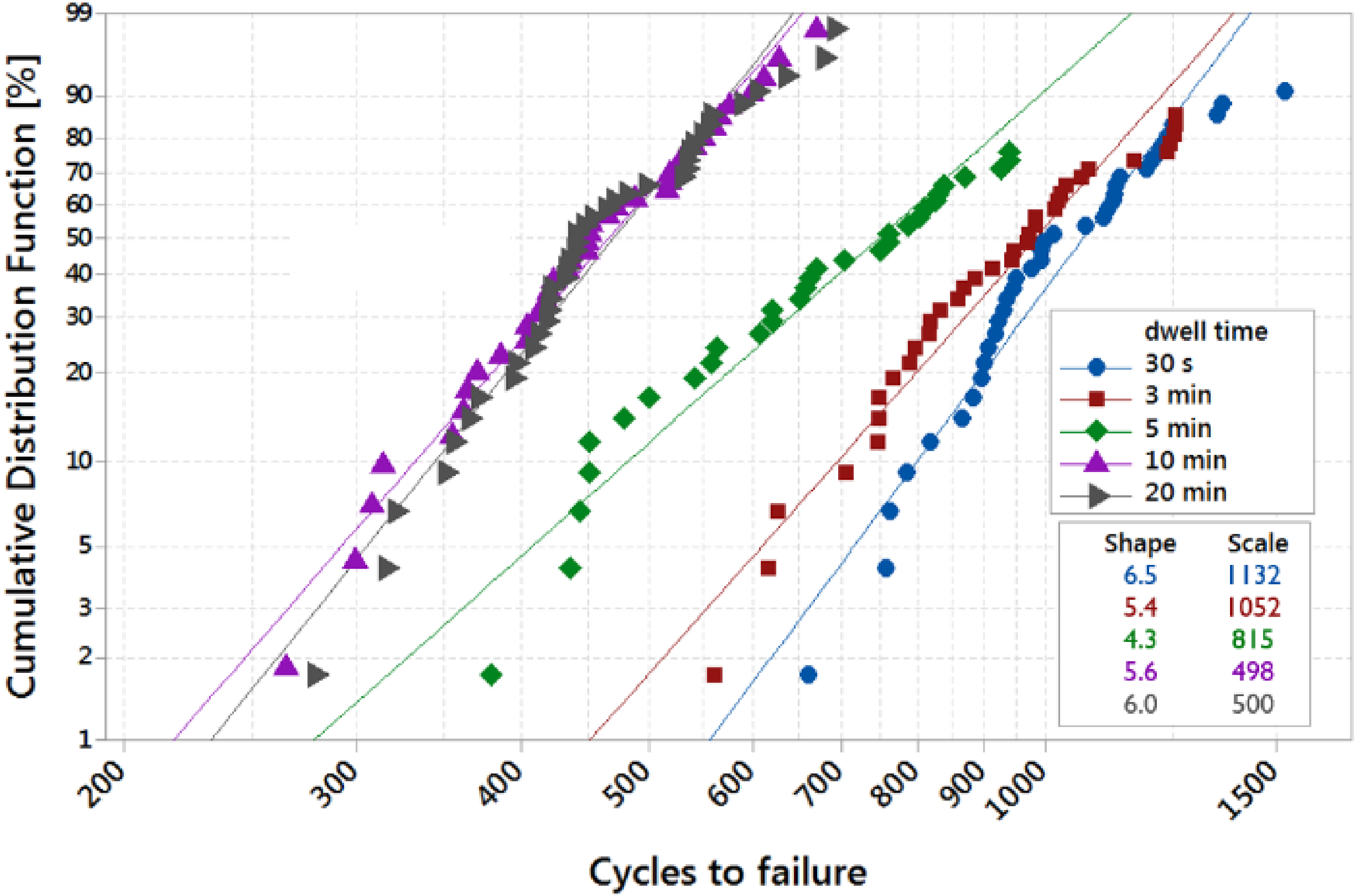
## ALSO A DIFFERENT STATISTICAL APPROACH

| | |
|---|---|
| System with 1 joint | Reliability: $R_1 = e^{-\left(\frac{t}{\mu}\right)^{\beta}}$ |
| System with 4 joints in parallel (cfr. Thermal Cycling) | Reliability: $R_4 = e^{-\left(\frac{t}{\mu_4}\right)^{\beta}}$ with $\mu_4 = \mu\left(\frac{1}{4}\right)^{1/\beta}$ |
| System with 16 joints (cfr 4 pt bending cycling) | Reliability: $R_{16} = e^{-\left(\frac{t}{\mu_{16}}\right)^{\beta}}$ with $\mu_{16} = \mu\left(\frac{1}{16}\right)^{1/\beta}$ |

➡ **$\mu_{16}/\mu_4 = 0.8$**

# 4PT BENDING EXPERIMENTS WITH VARYING DWELL TIME

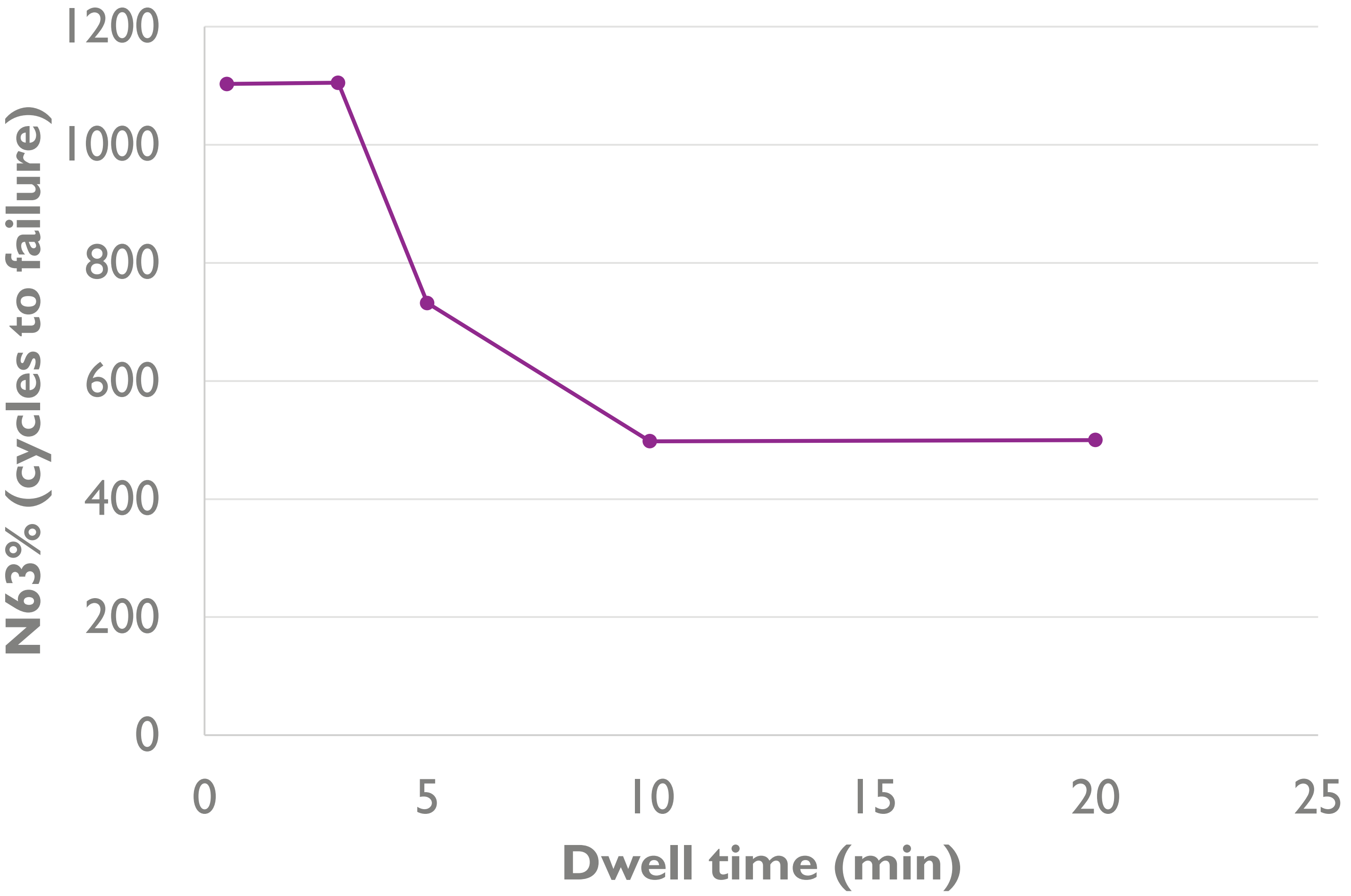
## WEIBULL RESULTS

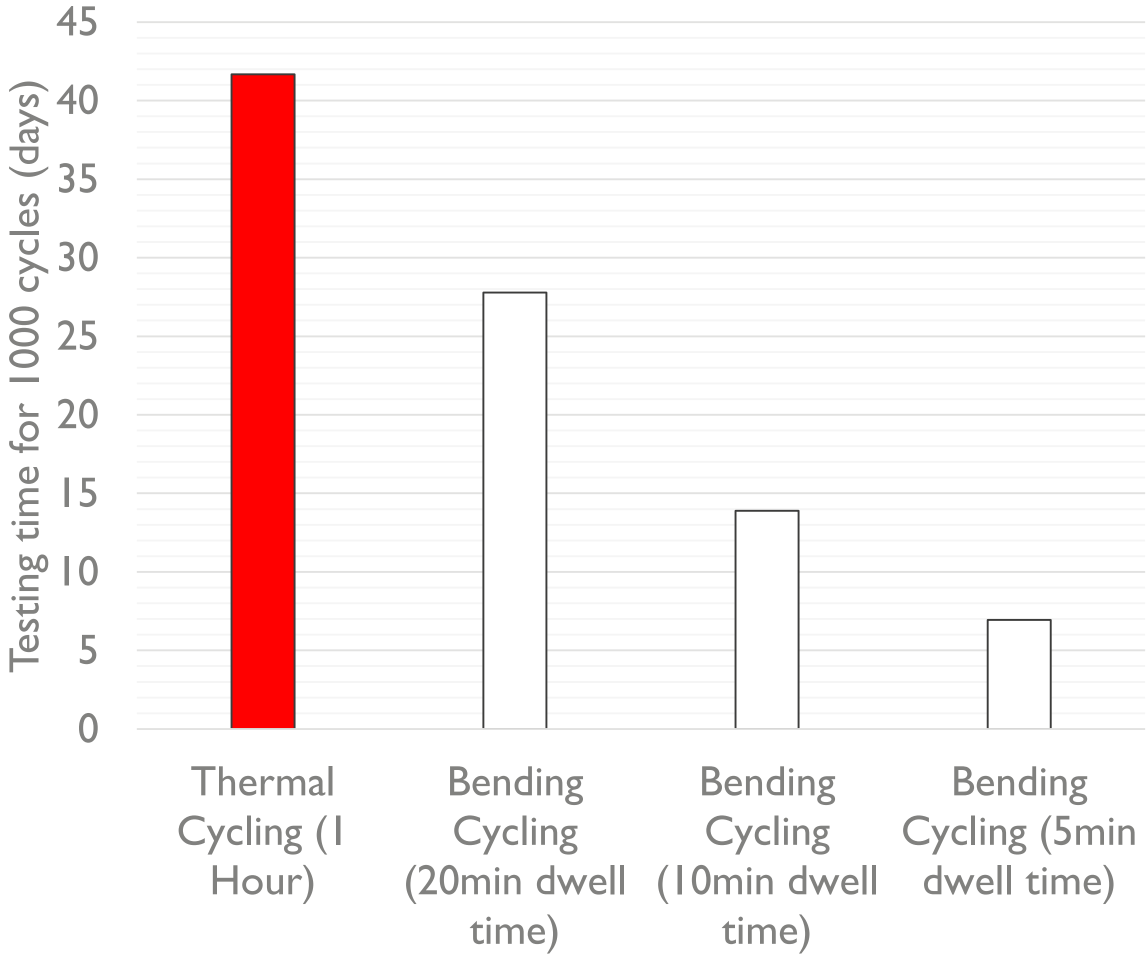


| Shape | Scale |
|---|---|
| 6.5 | 1132 |
| 5.4 | 1052 |
| 4.3 | 815 |
| 5.6 | 498 |
| 6.0 | 500 |

# 4PT BENDING EXPERIMENTS WITH VARYING DWELL TIME

- No difference between 10 and 20 minutes (is only valid for this temperature)
- Faster cycling doubles the life time (but also not more than that)





- Calculating the time needed for testing 1000 cycles (Figure 15), bending cycling with 10 minutes dwell time can reduce the testing time to **1/3** compared to thermal cycling

# CONCLUSIONS

4pt bending experiments have been performed on test boards with 24 soldered daisy chain WL-CSP's and results benchmarked with thermal cycling

- The same failure mode is generated (solder joint fatigue fractures)
- The joints fails much faster with 4pt bending for the same applied board strain (test @ constant higher temperature)
- With 4-pt bending cycling, the test time could be reduced by a factor of three. The technique even allows to further accelerate without the danger to initiate new failure modes.
- Be ware of the statistics: a higher number of equally loaded joints leads to lower life time of the daisy chain

# CONCLUSIONS (2)

Can the 4pt bending cycling fully replace the thermal cycling qualification tests?

- No, but it can reduce the total test time by pre-qualification of components and solder materials
- Suitable technique to derive acceleration factors
- Test can run in parallel with ThermalCycling (in order to have also the package warpage effects)

- This work is supported by several projects funded by Vlaio (Flemish Government)

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