PBA Design-for-eXcellence Guideline

EDM-D-010
Power Integrity

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The Electronics Design and Manufacturing Guidelines principles

The PBA Design-for-eXcellence (DfX) Guidelines are designed to provide all electronic supply chain actors involved in the design, qualification, industrialization and production of Printed Board Assemblies practical guidelines to master the multi-disciplinary hardware aspects of electronic module realization and operation in a cost-effective way. The PBA DfX Guidelines are not electrical design guidelines. The PBA DfX guidelines provide the electrical designer the boundary conditions of industrial electronic manufacturing technology and basic operational reliability. It is intended to support the development of cost-effective, reliable PBA with a short time-to-market requiring a minimum number of design iterations.
Some of the characteristics of the PBA DfX Guidelines are:

- The PBA DfX Guidelines are oriented towards the overall optimization of the hardware realization aspects of the final PBA based product.
- The guidelines refer to the relevant industry standards that are predominantly used in the international electronics industry such as those published by organizations as IPC and JEDEC. The guidelines do not replace industrial standards but define or recommend what options in the standards to use and will fill-in gaps if necessary. They provide the basis on which a company/product/product-line or application specific approach for design, industrialization and/or realization can be defined.
- Scientific argumentation and physical models form the basis of a large part of the guidelines and of the associated tools. This allows the use of the guidelines beyond the boundary of the users' experience domain. Therefore, it provides a powerful product and process innovation aid.
- The PBA DfX Guidelines will not specify, recommend or exclude specific brands of materials, components, suppliers or products. They will put forward minimal requirements on quality, physical and chemical properties and testing. They define and provide the DfManufacturing window for PBA realization.
- The PBA DfX Guidelines are based on verifiable physical models, standards and empirical data.

PBA DfM Guideline Scope

- This guideline focusses on the Power Integrity (PI) of a PBA. This guideline is complementary to the EMC guideline EDM-D-011 and the SI guideline EDM-D-009.
- This Power Integrity guideline provides a concise overview of a generic work-flow to obtain a low-impedance power distribution network on a PBA
- This guideline applies to all types (rigid, flex, flex-rigid) and IPC classes 1, 2 and 3 of PCB and PBA, both SnPb and leadfree soldered.

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1. Applicable Documents

This PBA DfM Guideline refers as part of the guideline to the most recent versions of the following documents and standards including their amendments.

EDM-D-009 Signal Integrity
EDM-D-011 Electro-Magnetic Compatibility(EMC)

2. Applicability of the PBA DfX Guideline EDM-D-010

- The recommendations given in the guideline are intended to help the user in making choices that improve the manufacturability, reliability, testability, etc., of the final PBA. These recommendations are of a generic nature. Therefore, in specific cases more optimal solutions may exist.
- Design specification takes precedence over this guideline.

3. Power Integrity

3.1. Design-for-Power Integrity goal and approach

3.1.1. Design for Power Integrity ensures that each component receives a constant power supply voltage by minimizing noise caused by the fast current changes of switching components that connect to the PDN. It aims at keeping high-frequency currents caused by fast-switching components close to these components.

3.1.2. Improper Design for Power Integrity leads to:
3.1.2.1. Ground bounce or Simultaneous Switching Noise
3.1.2.2. Eye diagram collapse (see Signal Integrity)
3.1.2.3. Unwanted radiation from e.g. cables connected to the PBA (see EMC)

3.1.3. Power Integrity is achieved by appropriate design of the Power Distribution Network (PDN) of the PBA. Based on application-specific requirements, the impedance of the PDN has to be lower than a target value from DC up to the highest-frequency-of-concern on the PBA as defined in Appendix A.

3.1.4. The first step is to specify the target impedance for each voltage rail.

3.1.5. The second step is to optimize the PDN by applying a good Voltage Regulator Module (VRM) together with a well-thought decoupling strategy on the PBA. Components especially designed for high-frequencies and mounted in the appropriate way form the basis of a successful decoupling strategy.

3.1.6. This guideline provides analytical formulas which can be used as first order estimates in the design of a PDN. To obtain a well-optimized PDN simulation based verification and optimization is required.

3.2. Specifying the target impedance

3.2.1. The following workflow to determine the target impedance for a specific voltage rail shall be applied to each voltage rail..

3.2.2. Determine the maximum transient current that is drawn from the voltage rail per connected component. If the transient current is not mentioned in the specification sheet of a component, use the following estimate:

$$I_{transient} \approx {}^{1}/_{2}\, I_{peak} \quad [1]$$

I_{peak} is the maximum current drawn by the component.

3.2.3 Determine the application dependent maximum acceptable voltage ripple (%) . The target impedance is obtained as: